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First Single-Chip Network Synchronization Solution Provides Ultra Precise Timing for 5G Radio Access Equipment

Combines integration and performance in one compact, low-power device supported by Microchip's widely deployed IEEE 1588 Precision Time Protocol (PTP) and synchronization algorithm software modules

CHANDLER, Ariz., July 29, 2021 (GLOBE NEWSWIRE) -- 5G technology requires time sources to be synchronized throughout a packet-switched network ten times more accurately than 4G requirements. Microchip Technology Inc. (**Nasdaq: MCHP**) now makes it possible to achieve 5G performance with the first single-chip, highly integrated, low-power, multi-channel integrated circuit (IC) coupled with the company's widely adopted and reliable IEEE® 1588 Precision Time Protocol (PTP) and clock recovery algorithm software modules.

"Our newest [ZL3073x/63x/64x network synchronization platform](#) implements sophisticated measure, calibrate and tune capabilities, thereby significantly reducing network equipment time error to meet the most stringent 5G requirements," said Rami Kanama, vice president of Microchip's timing and communications business unit. "A uniquely flexible architecture for implementing the necessary channel density as well as high-performance, low-jitter synthesizers help simplify the design of timing cards, line cards, Radio Units (RU), Centralized Units (CUs) and Distributed Units (DUs) for 5G Radio Access Networks (RAN)."

Microchip's measure, calibrate and tune capabilities ensure 5G systems achieve International Telecommunication Union – Telecommunication (ITU-T) Standard G.8273.2 Class C (30ns max|TE|) and the emerging Class D (5ns max|TE|) time error requirements. The architecture provides flexibility, offering up to five independent Digital Phase Locked Loop (DPLL) channels while consuming only 0.9W of power in a compact 9 x 9-millimeter package that simultaneously reduces board space, power and system complexity.

With five ultra-low-jitter synthesizers, this latest platform offers 100 femtosecond (fs) root mean square (rms) jitter performance required by high-speed interfaces in the latest 5G RU, DU and CU systems.

Microchip's network synchronization platform software includes its ZLS30730 high-performance algorithm coupled with its ZLS30390 IEEE 1588-2008 protocol engine. Both are widely deployed in 3G, 4G and 5G networks with precise timing capabilities.

Microchip's ZL3073x/63x/64x network synchronization platform combines seamlessly with the company's family of precision 5G oscillators – for example, the [OX-601 Oven Controlled Crystal Oscillator](#) (OCXO) – to offer 5G network operators a total system solution.

The company's extensive portfolio of timing and clock solutions include clock generation, fanout buffer and jitter attenuator solutions as well as quartz and MEMS oscillators is complemented by a broad family of Ethernet physical layer (PHY) devices.

Development Tools

Microchip offers a graphical user interface (GUI) and evaluation board along with application notes and other design-in support tools.

Availability

Microchip's ZL3073x/63x/64x network synchronization platform is available in production quantities and offered with IEEE 1588 PTP and algorithm software modules, which are provided through license terms for download.

For additional information, contact a Microchip sales representative or authorized worldwide distributor.

Resources

High-res images available through Flickr or editorial contact (feel free to publish):

- Application image: <https://www.flickr.com/photos/microchiptechnology/51306164402/>
- Block diagram: <https://www.flickr.com/photos/microchiptechnology/51307098488/>

About Microchip Technology

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