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Microchip Introduces First Clock Buffers to Meet DB2000Q/QL Standards plus PCIe Gen 4 and Gen 5 Low Jitter Specifications

20-output PCIe clock buffer is ideal for next-generation servers, data centers, storage devices and other PCIe applications

CHANDLER, Ariz., June 25, 2019 (GLOBE NEWSWIRE) -- As data centers migrate to greater bandwidth and faster infrastructure, the need for higher performance timing devices becomes critical. Four new 20-output differential clock buffers that exceed PCIe® Gen 5 jitter standards for next-generation data center applications are now available from Microchip Technology Inc. **(Nasdaq: MCHP)**. The **ZL40292** (85Ω termination) and **ZL40293** (100Ω termination) are specifically designed to meet the new DB2000Q specification while the **ZL40294** (85Ω termination) and **ZL40295** (100Ω termination) are designed to meet the DB2000QL industry standard. All are ideally suited for next-generation servers, data centers, storage devices and other PCIe applications. These new devices also meet PCIe Gen 1, 2, 3 and 4 specifications.

Each buffer is an ideal complement to chipsets where distributed clocks are required across several peripheral components, such as Central Processing Units (CPUs), Field Programmable Gate Arrays (FPGAs) and Physical layers (PHYs) in data center servers and storage devices, along with many other PCIe applications. The devices' low additive jitter of approximately 20 femtoseconds (~20 fs) far exceeds the DB2000Q/QL specification of 80 femtoseconds (80 fs). This provides designers large margins to meet tight timing budgets while achieving increasing data rates. These devices will minimize jitter when distributing clocks to up to 20 outputs, thereby maintaining the integrity and quality of the clock signal through the buffer.

The new buffers achieve low power dissipation and contribute significant savings to power budgets by using Low-Power High-Speed Current Steering Logic (LP-HCSL). Compared to standard HCSL, LP-HCSL consumes one third of the power, leading to a significant decrease in power consumption. This feature also gives customers the ability to drive longer traces on their board, improving signal routing while reducing components and board space. The ZL40292, for example, can eliminate up to 80 termination resistors (four per output) compared to traditional HCSL buffers.

"Microchip provides the broadest clock and timing portfolio in the industry and continues to develop solutions to address demanding next-generation networking applications, such as higher speed data center and enterprise infrastructure," said Rami Kanama, vice president of Microchip's timing and communications business unit. "Customers who are seeking DB2000Q- and DB2000QL-compliant clock buffers can begin their designs now because of Microchip's early introduction and the superior performance of PCIe Gen 5 devices, offering engineers greater design margins and peace of mind."

Pricing and Availability
The ZL40292 and ZL40293 are available now for sampling and in volume production in 72-pin 10 x 10 mm QFN packages. The ZL40294 and ZL40295 are available now for sampling in the 80-pin 6 x 6 QFN packages. For pricing and additional information, contact a Microchip sales representative, authorized worldwide distributor or visit Microchip's website. To purchase products mentioned here or get additional information visit our **purchasing portal** or contact a Microchip authorized distributor.

Resources
High-res images available through Flickr or editorial contact (feel free to publish):

- Application image: **www.flickr.com/photos/microchiptechnology/48039160482/sizes/l**
- Chip graphic: **www.flickr.com/photos/microchiptechnology/48039101208/sizes/l**

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