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AMD to Boost Performance for Everyday Compute-Intense Multimedia, Security and High Performance Computing Applications through New Extensions to x86 Instruction Set

New Instruction Set "SSE5" Continues Tradition of AMD x86 Innovation, Including 3DNow!, AMD x86-64 Architecture, AMD Virtualization and Light-Weight Profiling Specification

SUNNYVALE, Calif.--(BUSINESS WIRE)--

AMD (NYSE:AMD) today announced further plans to innovate the x86 architecture by introducing SSE5, a new extension of the x86 instruction set that is designed to allow software developers to simplify code and achieve greater efficiency for the most performance-hungry applications. SSE5 will give developers additional capabilities to help maximize the performance of applications that have daily impact on consumers and enterprises, including high performance computing, multimedia and security applications. By making the SSE5 specification available to developers today, AMD expects to ease the adoption of the new instructions for tool providers and software vendors who develop these performance-intense applications.

"Chip advancements and software improvements go hand-in-hand, to the benefit of consumers and enterprises alike," said Phil Hester, senior vice president and chief technology officer, AMD. "The impact of our designs are best realized when AMD-based servers, PCs and devices enable software to more effectively solve every-day problems and enhance every-day experiences. By announcing our plans to add SSE5 instructions to the x86 instruction set -- and by making the specification available today -- we are enabling open and collaborative software innovation that will bring AMD's advancements to life for our customers and end-users."

As the industry's focus is shifting from processor speeds to increasing power efficiency, the number of instructions executed per second on one processor core remains relatively constant. As a result, both software and hardware vendors must pursue new approaches to improving computing performance.

AMD is once again helping advance this process by making technical details available to the software developer community early, to foster an industry dialogue and solicit feedback. For example, AMD released an early version of the AMD Virtualization(TM) specification in 2005, at the time codenamed "Pacifica," to the benefit of that technology's further development. Additionally, AMD recently released the Light-Weight Profiling proposal, which is designed to

enable software developers to fully leverage the benefits of multi-core computing. The early release of the SSE5 specification to the software developer community follows AMD's philosophy of open collaboration, a model that effectively drove x86, 64-bit computing to the masses.

"PGI's goal is to provide high-performance, cross-platform, production-quality parallel compilers and software development tools to the developer community," said Douglas Miles, director, The Portland Group. "We are working closely with AMD to enable developers to quickly and easily leverage the SSE5 instruction set to enhance high performance computing, and the multi-core and multi-media capability of their software applications."

Multi-core processor technology and the integration of specialized co-processors are effective methods for extending performance limits. Equally important is enabling the ability to maximize the efficiency of each core by reducing the total number of instructions needed to achieve the same result. SSE5 helps maximize the output of each instruction and consolidates code base by introducing functionality previously only found in specialized, high-performance architectures, to the x86 platform:

-- 3-Operand Instructions

A computing instruction is executed by applying a mathematical or logical function to operands, or inputs. By increasing the number of operands an x86 instruction can handle from 2 to 3, SSE5 enables the consolidation of multiple, simple instructions into a single, more effective instruction. The ability to execute 3-Operand Instructions is currently only possible on certain RISC architectures.

-- Fused Multiply Accumulate

The 3-Operand Instruction capability enables the creation of new instructions which efficiently execute complex calculations. The Fused Multiply Accumulate instruction combines multiplication and addition to enable iterative calculations with one instruction. The simplification of the code enables rapid execution for more realistic graphics shading, rapid photographic rendering, spatialized audio, complex vector mathematics and other performance-intense applications.

The SSE5 specification, which is being made available to the developer community today at http://developer.amd.com/SSE5, will be implemented in products based on AMD's next-generation "Bulldozer" core, available in 2009.

What is SSE?

Introduced in 1999, SSE (Streaming SIMD Extensions) is a SIMD (Single Instruction, Multiple Data) instruction set for the x86 architecture, designed to increase software performance through the use of special instructions that can operate on multiple pieces of data at one time.

About AMD

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