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Microchip and Acacia Collaborate to Enable Optimized Terabit-Scale Data Center Interconnect Systems

The companies enable an interoperable coherent optics ecosystem that can help streamline the development of data center interconnect and metro transport systems

CHANDLER, Ariz., Aug. 13, 2024 (GLOBE NEWSWIRE) -- The latest data center architectures and increased traffic are driving higher bandwidth requirements between data centers. To address this challenge, system developers must streamline the development of a new generation of 1.2 Tbps (1.2T) transport solutions across a wide range of client configurations. This requires that today's terabit-scale Ethernet PHY devices and coherent optical modules interoperate with each other in Data Center Interconnect (DCI) and metro transport networks. Microchip Technology (**Nasdaq: MCHP**) today announces that it has worked with Acacia to demonstrate the fourth generation of interoperability between Microchip's [META-DX2](#) Ethernet PHY family and Acacia's [Coherent Interconnect Module 8](#) (CIM 8).

The two companies' interoperable devices enable low-power, bandwidth-optimized, scalable solutions for pluggable optics in DCI and transport networks. They deliver three key benefits as they jointly enable high-capacity, multi-rate muxponders for optical transport platforms:

- **Optimized DCI bandwidth:** The META-DX2 family, through its META-DX2+ PHY, uses its unique Lambda Splitting feature to split 400 GbE or 800 GbE clients across multiple wavelengths driven by the CIM8 modules. This maximizes the capacity between data centers in rate configurations such as 3x800 GbE over 2x1.2 Tbps waves or 5x400 GbE over 2x1.0 Tbps waves.
- **Reduced design risk:** Microchip and Acacia have jointly verified successful SerDes interoperation at up to 112G per lane for Ethernet and OTN clients, which reduces design validation and system qualification requirements.
- **Better support for full bandwidth, multi-rate operation:** The META-DX2+ crosspoint and gearbox functions enable 100 GbE to 800 GbE client modules to connect with full bandwidth to CIM8 modules.

"This interoperability extends a long-established partnership with Acacia to help accelerate and optimize the build-out of cloud computing and AI-ready optical networks while reducing development risk for our customers," said Maher Fahmi, vice president for Microchip's communications business unit. "Our META-DX2 is the first solution of its kind to integrate 1.6T of encryption, port aggregation and Lambda Splitting into the most compact 112G PAM4 device in the market."

"With Acacia's CIM 8 coherent modules verified to interoperate with Microchip's META-DX2 devices, we see this as a robust solution that reduces system time-to-market," said Markus

Weber, senior director DSP product line management of Acacia. “The compact size and power efficiency of our CIM 8 coherent modules were designed to help network operators deploy and scale capacity of high-bandwidth DWDM connectivity between data centers and throughout transport networks.”

Resources

High-res images available through Flickr or editorial contact (feel free to publish):

- Application image:
www.flickr.com/photos/microchiptechnology/53725782078/sizes//

About Microchip Technology:

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