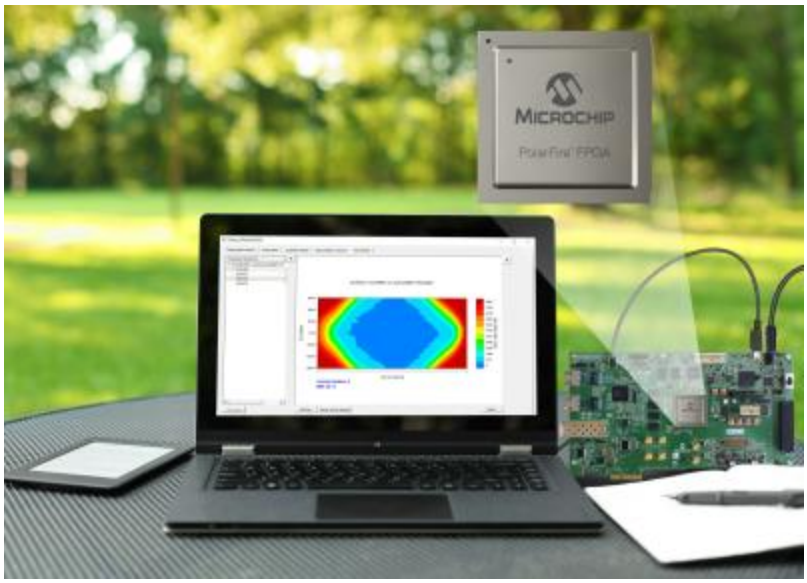
January 29, 2019

Microchip's First Libero SoC Design Suite Release Boosts FPGA Designer Productivity and Delivers One Unified Design Suite for Latest Families

New version delivers significant productivity gains while marking major production milestones for the low-power PolarFire™ FPGA family

CHANDLER, Ariz., Jan. 29, 2019 /PRNewswire/ -- As each new generation of devices scale, Field Programmable Gate Array (FPGA) designs are increasing in complexity and resource utilization, making designer productivity essential to accelerating time to market. Microchip Technology Inc. (Nasdaq: MCHP), via its Microsemi Corporation subsidiary, today announced the release of **Libero SoC version 12.0,** delivering new gains in runtime and quality of results, as well as one unified design suite for all the company's latest-generation FPGA families, including new production releases of PolarFire FPGAs.



Libero SoC v12.0 reduces design flow runtimes and, with the improved quality of results, it provides results in fewer design iterations and improves customer productivity. By upgrading to Libero SoC v12.0, designers will see runtime reduction of 60 percent for timing, 25 percent for place and route and 18 percent for power results. They will also see an average increase of four percent in quality of results for larger designs and a 10 percent improvement for the PolarFire MPF300/TS-1 device.

"Libero SoC v12.0 is the result of our determination to offer a comprehensive, easy-to-adopt, easy-to-learn FPGA design suite," said Rajeev Jayaraman, vice president of software for the FPGA business unit at Microchip's Microsemi subsidiary. "This latest release is focused on

delivering the many essential elements needed for efficient design implementation, while further enabling the growing adoption of the low-power PolarFire family across each of our key market segments."

Libero SoC v12.0 is being released simultaneously with the production release of the PolarFire MPF100T, PolarFire MPF200T and PolarFire MPF300T devices. The release includes production timing and power for PolarFire MPF300T-1 devices, as well as support for two new industry-leading devices for the aerospace and defense market segments—the low-power, radiation-tolerant RT4G150L, which offers 25 percent savings for standard speed grade; and military-grade support for the SmartFusion2 M2S150T/S FCV484 device.

One unified design suite for PolarFire, IGLOO2, SmartFusion2 and RTG4 FPGAs eliminates the need for designers to qualify multiple pieces of software when working across product families. Libero SoC v12.0 now supports FPGA Hardware Breakpoint (FHB) for RTG4 and PolarFire devices, PCIe debug support for PolarFire and continuous transceiver eye monitoring using SmartDebug. The new release also improves Double Date Rate (DDR) memory performance by an average of 29 percent in high-effort mode and 39 percent in regular-effort mode. Enhanced Tool Command Language (TCL) support enables a much-requested feature where customers can run the entire design flow on the command line if they so choose.

Availability
Microchip's Libero SoC v12.0 design suite is available now to support customers designing with its PolarFire, IGLOO®2, SmartFusion®2 and RTG4™ FPGAs. For more information on licensing, visit https://www.microsemi.com/product-directory/design-resources/1711-licensing or contact SoC_Tech@microsemi.com. The software can be downloaded at https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads.

Resources
High-res images available through Flickr or editorial contact (feel free to publish):

- Application image: https://www.flickr.com/photos/microchiptechnology/45991534435

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