August 14, 2020

Media Alert: Intel at Hot Chips 2020

SANTA CLARA, Calif.--(BUSINESS WIRE)-- Join Intel at Hot Chips, a conference on high-performance microprocessors and related integrated circuits, where Raja Koduri, senior vice president, chief architect and general manager of Architecture, Graphics and Software, will deliver a keynote presentation explaining the opportunities for hardware-software co-design. Together with partners and customers, Intel is building the trusted foundation for computing in a data-centric world.

Hot Chips 2020
When: Sunday, Aug. 16 — Tuesday, Aug 18, 2020
Where: Virtual Event
Registration

Keynote: No Transistor Left Behind
Raja Koduri
When: Monday, Aug. 17, 2-3 p.m.
While silicon technology scaled exponentially over the past few decades, the breadth and depth of the software stack scaled at a much faster rate than could have been predicted by Moore's Law, bringing inefficiencies and leaving plenty of room for increasing performance. In this keynote, Raja Koduri will explore opportunities in hardware-software co-design from the edge to the cloud to fully leverage the transistors that are left behind by the incredible pace of software change at the top of the stack.

Towards a Large-Scale Quantum Computer Using Silicon Spin Qubits
James S. Clarke
When: Sunday, Aug. 16, 3:15-3:45 p.m.
James S. Clarke, director of quantum hardware at Intel, will present progress toward the realization of a 300mm Si-MOS based spin qubit device in a production environment. In addition, this talk will focus on a key bottleneck to moving beyond today's few-qubit devices: the interconnect scheme and control of a large quantum circuit. To address this bottleneck, at Intel we have developed customized control chips, optimized for performance at low temperature, with a goal of simplifying wiring of quantum systems and replacing the racks and racks of discrete electrical components.

Next Generation Intel Xeon(R) Scalable Server Processor: Icelake-SP
Irma Esmer Papazian
When: Monday, Aug. 17, 9:30-11:30 a.m.
Irma Esmer Papazian, senior principal engineer in architecture at Intel, will present on the next generation Intel® Xeon™ processor (code named "Icelake-SP"), a general-purpose server processor designed to bring significant performance boost over prior-generation Xeon processors. Icelake-SP is the first Xeon server implemented on Intel 10nm processor technology and is targeted for the end of 2020. Irma will describe new enhancements to Icelake-SP, including ISA, security technologies and core microarchitecture improvements,

diving into their use and impact in server application. She will also highlight key features, microarchitecture insights and performance trends of Icelake-SP not shared previously.

Inside Tiger Lake: Intel's Next Generation Mobile Client CPU
Xavier Vera
When: Monday, Aug. 17, 12-1 p.m.
Xavier Vera, principal engineer and SoC/performance power architect at Intel, will lead a discussion on Tiger Lake, Intel's next generation mobile client CPU. Tiger Lake provides the best performance and battery life Intel has ever offered for mobile content creation, productivity and gaming usages. The new high-performance core in Tiger Lake is called Willow Cove, which adds enhanced security features to help protect against return-oriented programming attacks along with increases in performance via frequency push and L2 cache size increases. Intel® Xe-LP is the new graphics engine within Tiger Lake that increases the maximum number of execution units from 64 to 96. Xavier will cover how Tiger Lake was able to achieve significant gains in performance and drive competitive battery life.

The Xe GPU Architecture
David Blythe
When: Monday, Aug. 17, 5-6:30 p.m.
David Blythe, Intel senior fellow and director of Graphics Architecture, will discuss Xe, Intel's next-generation GPU architecture. Xe was designed for scalability – spanning teraflop to petaflop compute performance – and is slated for use in multiple Intel products including Tiger Lake Client SoC and HPC GPU Ponte Vecchio. In this presentation, he will explain the principles behind Xe configurability and scalability and its many efficiency enhancements, as well as new capabilities, including hardware acceleration support for ray tracing, matrix/tensor processing and multidie/multipackage connectivity. Blythe will then delve into details for one configuration of the architecture, Xe-LP, employed in lower TDP product segments.

Agilex Generation of Intel FPGAs
Ilya Ganusov and Mahesh A. Iyer
When: Tuesday, Aug. 18, 8:30-10 a.m.
Ilya Ganusov, senior principal engineer and director of Programmable Architecture at Intel, and Mahesh A. Iyer, Intel fellow in the Data Platforms Group and chief architect and technologist of Electronic Design Automation, will provide an in-depth technical disclosure of Intel's next-generation Agilex™ FPGA platform. Agilex™ FPGAs deliver over 40% higher peak performance and use 40% less power, on average, over prior generation Stratix®10 FPGAs. Details on volume production shipment on engineering samples of Agilex™ FPGAs will be revealed in the presentation.

Tofino2 – A 12.9Tbps Programmable Ethernet Switch
Anurag Agrawal and Changhoon Kim
When: Tuesday, Aug. 18, 10:30 a.m.-12:30 p.m.
In this presentation, Anurag Agrawal, senior principal engineer in the Barefoot Division of the Data Center Group, and Changhoon Kim, Intel fellow in the Connectivity Group and chief technical officer of applications in the Barefoot Switch Division, will describe Tofino2, a 12.9Tbps fully-programmable switch silicon that is an evolution of the original Tofino architecture in both speed and capability. Enhancements to Tofino2 include an increase in fungible resources and the addition of several novel primitives to help users realize new

types of networking protocols and functions, such as advanced telemetry, advanced congestion control and flexible scheduling.

About Intel

Intel (Nasdaq: INTC) is an industry leader, creating world-changing technology that enables global progress and enriches lives. Inspired by Moore's Law, we continuously work to advance the design and manufacturing of semiconductors to help address our customers' greatest challenges. By embedding intelligence in the cloud, network, edge and every kind of computing device, we unleash the potential of data to transform business and society for the better. To learn more about Intel's innovations, go to newsroom.intel.com and intel.com.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors.

Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit www.intel.com/benchmarks.

Statements in this document that refer to future plans or expectations are forward-looking statements. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings release and SEC filings at www.intc.com.

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