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Microchip Unveils Industry's Most Compact 1.6T Ethernet PHY with Up to 800 GbE Connectivity for Cloud Data Centers, 5G and AI

META-DX2L enables routers, switches and line cards to double their bandwidth by transitioning to 112G PAM4 interface rates

CHANDLER, Ariz., Sept. 08, 2021 (GLOBE NEWSWIRE) -- Routers, switches and line cards need higher bandwidth, port density and up to 800 Gigabit Ethernet (GbE) connectivity to handle escalating data center traffic driven by 5G, cloud services and Artificial Intelligence (AI) and Machine Learning (ML) applications. To deliver the higher bandwidth, these designs need to overcome the signal integrity challenges associated with the industry's transition to the 112G (gigabits per second) PAM4 Serializer/Deserializer (SerDes) connectivity that is needed to support the latest pluggable optics, system backplanes and packet processors. These challenges can now be overcome with the industry's most compact, 1.6T (terabits per second), low-power PHY (physical layer) solution from Microchip Technology Inc. (**Nasdaq: MCHP**) with its [PM6200 META-DX2L](#) that reduces power per port by 35 percent compared to its 56G PAM4 predecessor, META-DX1, the industry's first terabit-scale PHY solution.

"The industry is transitioning to a 112G PAM4 ecosystem for high-density switching, packet processing, and optics," said Bob Wheeler, principal analyst for networking at The Linley Group. "Microchip's META-DX2L is optimized to address these demands by bridging line cards to switch fabrics and multi-rate optics for 100 GbE, 400 GbE and 800 GbE connectivity."

With its high-density 1.6T bandwidth, space-saving footprint, 112G PAM4 SerDes technology, and support for Ethernet rates from 1 to 800 GbE, Microchip's META-DX2L Ethernet PHY is an industrial-temperature-grade device that offers the connectivity versatility to maximize design reuse across applications ranging from a retimer, gearbox or reverse gearbox to a hitless 2:1 multiplexor (mux). Highly configurable crosspoint and gearbox features make full use of a switch device's I/O bandwidth to enable the flexible connections necessary for multi-rate cards that support a wide range of pluggable optics. The PHY's low-power PAM4 SerDes enables it to support the next-generation infrastructure interface rate for cloud data centers, AI/ML compute clusters, 5G, and telecom service provider infrastructure, whether over long-reach direct attach copper (DAC) cables, backplanes, or connections to pluggable optics.

"For the 56G generation we introduced the industry's first terabit PHY, META-DX1, and now we have followed with an equally transformative 112G solution that delivers the capabilities system developers need to solve today's new challenges posed by cloud data centers, 5G networking, and AI/ML compute scale-out," said Babak Samimi, vice president for Microchip's communications business unit. "By delivering up to 1.6T of bandwidth within a

low-power architecture and in the smallest footprint, the META-DX2L PHY doubles the bandwidth of previous solutions on the market while establishing a new level of power efficiency.”

META-DX2L is offered in the industry’s smallest package size, 23 x 30 millimeter (mm), which enables the space savings necessary to deliver the line card port densities demanded by hyperscalers and system developers. Product highlights include:

- Dual 800 GbE, Quad 400 GbE and 16x 100/50/25/10/1 GbE PHY
- Supports Ethernet, OTN, and Fibre Channel data rates
- Supports proprietary data rates for AI/ML applications
- Integrated 2:1 hitless mux enables high availability/protection architectures
- Highly configurable crosspoint supporting multi-rate services on any port
- Constant latency, enabling IEEE 1588 Class C/D PTP at the system level
- FEC termination, monitoring and conversion between various interface rates
- 32 long-reach (LR) capable 112G PAM4 SerDes with programmability to optimize power vs. performance
- Support for DAC cables, including auto-negotiation and link training
- Industrial-temperature-range support, enabling deployments in outdoor environments
- Complete Software Development Kit (SDK) with hitless upgrade and warm restart capabilities and compatible with the field-proven META-DX1 SDK

Microchip provides a full set of design-in collateral, reference designs, and evaluation boards to support customers building systems with META-DX2L devices. In addition to Ethernet PHY technology, Microchip also provides system vendors with a total system solution including PolarFire® FPGAs, the ZL30632 high-performance PLL, oscillators, voltage regulators, and other components that have been pre-validated as a system with META-DX2L to help bring designs to production faster.

Product Availability

Initial META-DX2L devices are expected to sample during the fourth calendar quarter of 2021. For additional information visit the [PM6200 META-DX2L](#) web page or contact a Microchip sales representative.

Resources

High-res images available through Flickr or editorial contact (feel free to publish):

- Application image:
www.flickr.com/photos/microchiptechnology/51374945989/sizes/l/

About Microchip Technology

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