

Investor Webinar

DCAI Business Update

John Pitzer

Corporate Vice President
Investor Relations

The Intel logo is displayed in white lowercase letters on a white square background. To the left of the square are three overlapping squares in shades of blue, arranged in a staircase pattern.

intel.

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- Future node performance and other metrics, including power and density, are projections and are inherently uncertain and, in the case of other industry nodes, are derived from or estimated based on publicly available information. Intel's node numbers do not represent the actual dimension of any physical feature on a transistor or structure. They also do not pinpoint a specific level of improvement in performance, power or area, and the magnitude of a decrease from one node number to the next is not necessarily proportionate to the level of improvement in one or more metrics. Historically, new Intel node numbers were based solely on improvements in area/density; now, node numbers generally reflect a holistic assessment of improvement across metrics and can be based on improvement in one or more of performance, power, area, or other important factors, or a combination, and will not necessarily be based on area/density improvement alone.
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Presenters



Sandra Rivera

Executive Vice President
General Manager,
Data Center & AI Group



Greg Lavender

Senior Vice President, CTO
General Manager, Software and
Advanced Technology Group



Lisa Spelman

Corporate Vice President
General Manager,
Xeon Products

DCAI Business Update Webinar

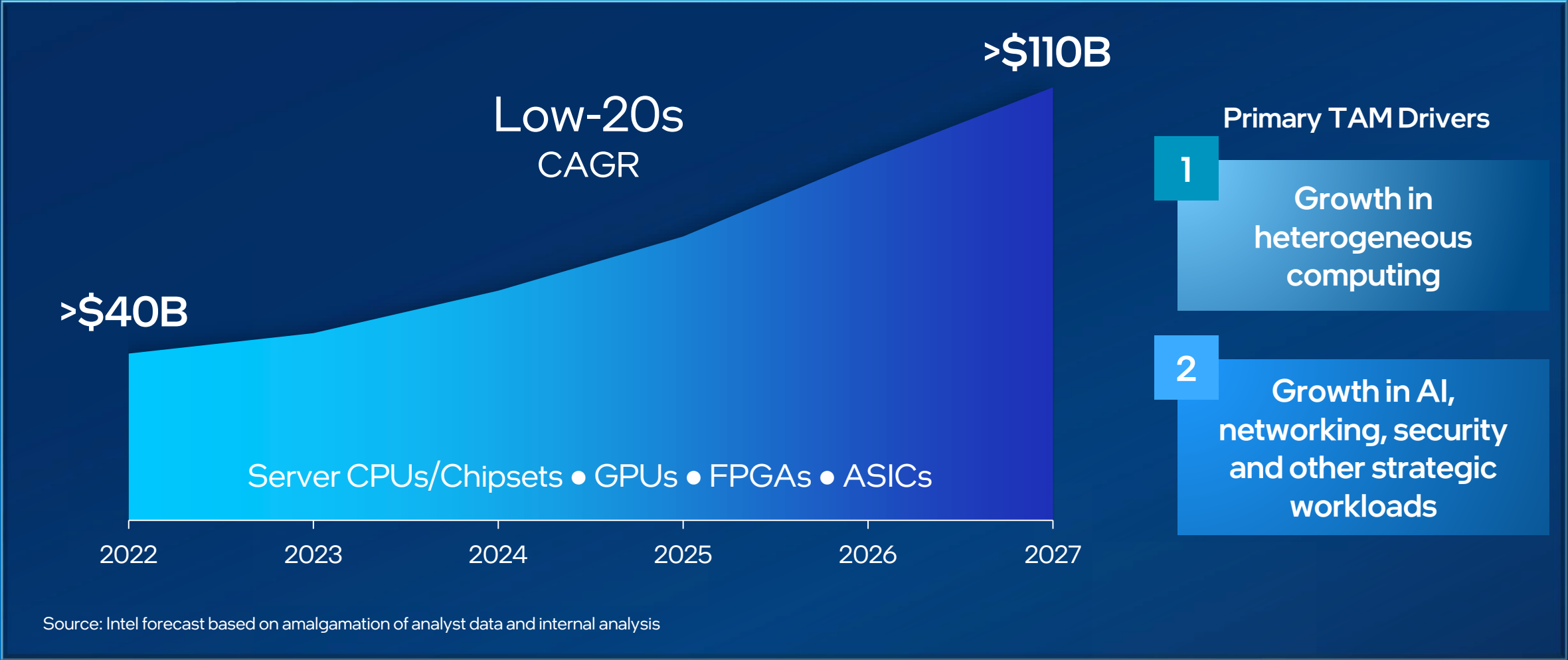
Data Center TAM Update: Sandra Rivera

Roadmap Update: Sandra Rivera & Lisa Spelman

Winning in AI: Sandra Rivera & Greg Lavender

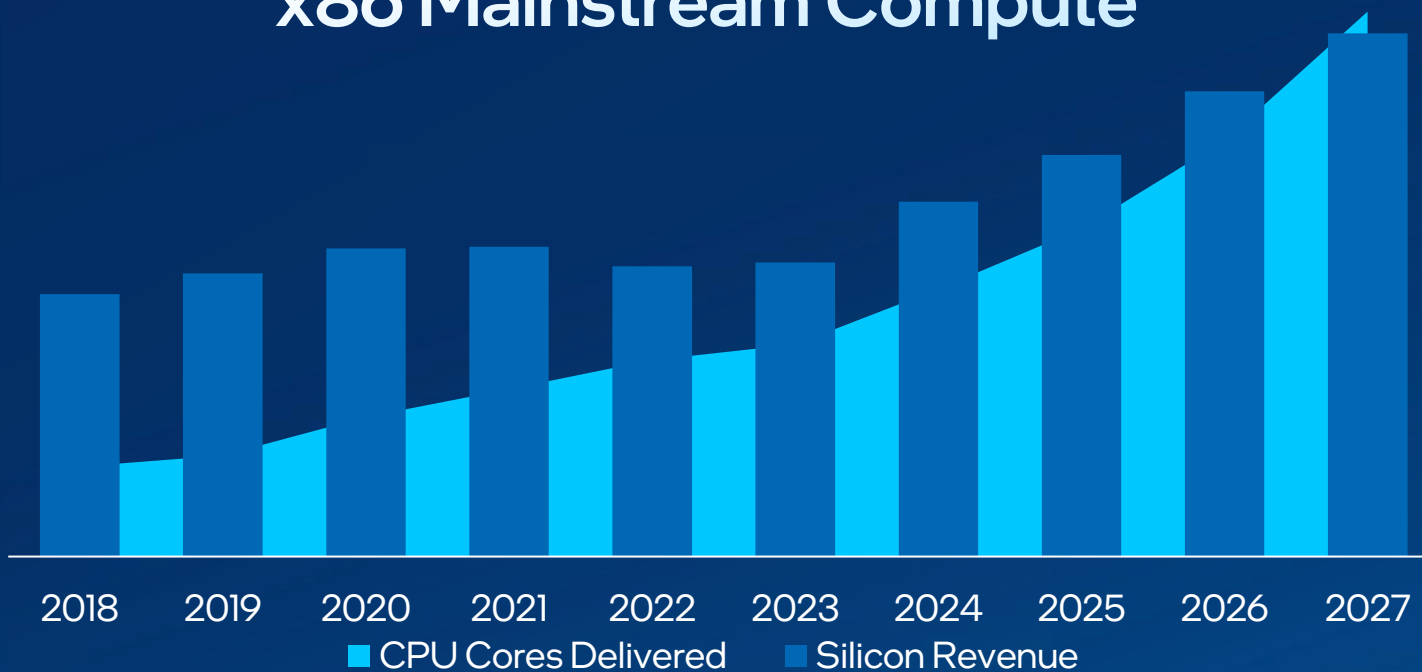
Wrap Up and Q&A: Sandra Rivera

DCAI Silicon TAM Opportunity



Silicon Revenue Will Follow CPU Core Trends

x86 Mainstream Compute



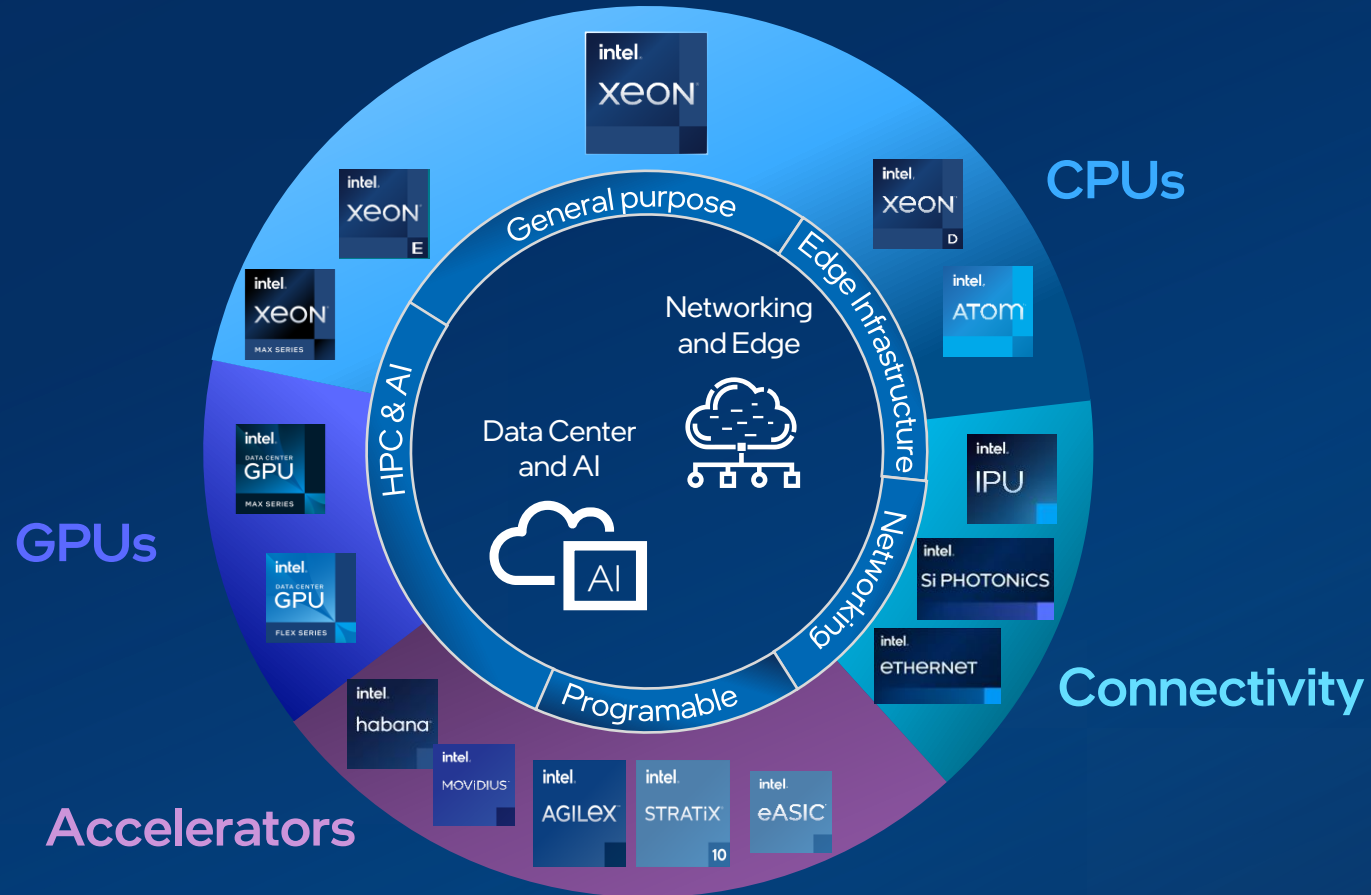
Source: Intel forecast based on amalgamation of analyst data and internal analysis

- Compute demand has strong growth trajectory
- Xeon core growth increasing at a faster rate than previous generations
- Delivering customer value through CPU cores, built-in acceleration & heterogenous computing

Mainstream Compute Cores Growing at Mid-20s CAGR

Delivering the Broadest Portfolio

Driving Innovation from the Cloud, through the Network to the Intelligent Edge

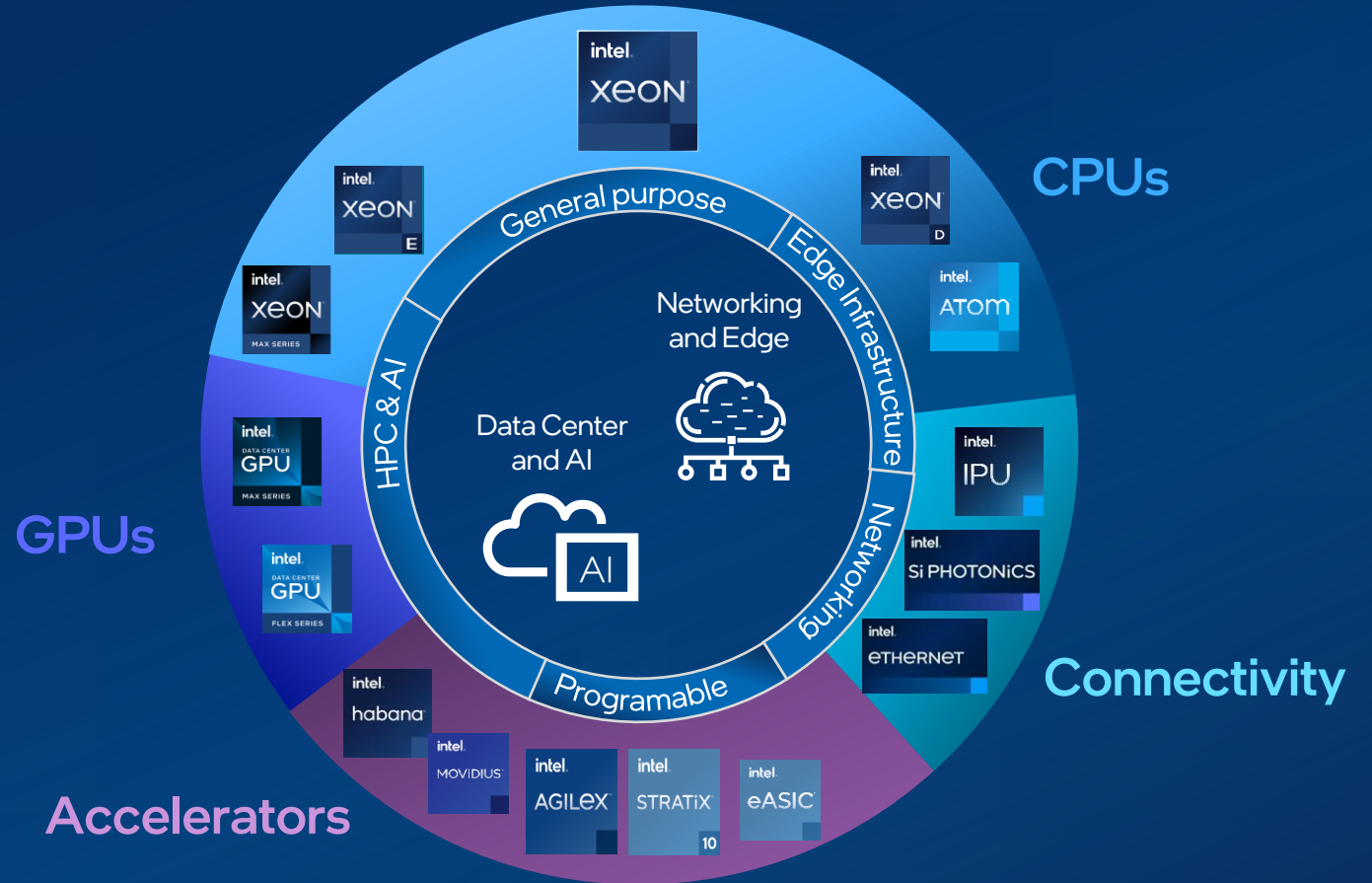


Delivering the Broadest Portfolio

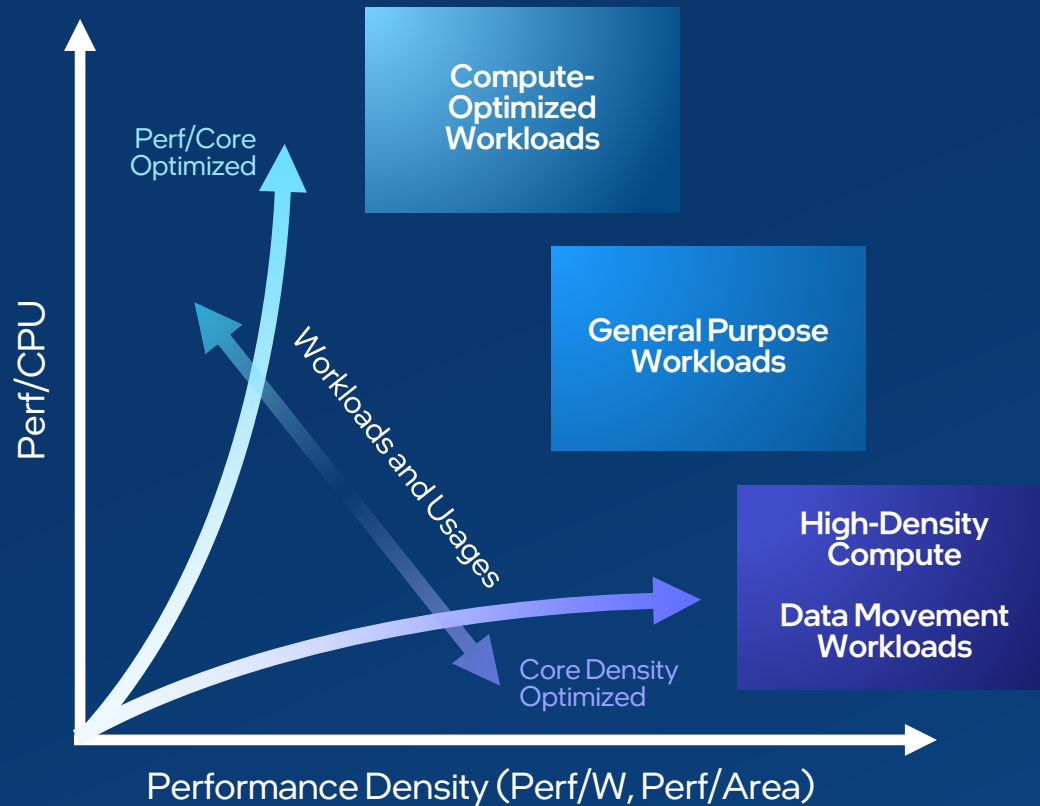
Driving Innovation from the Cloud, through the Network to the Intelligent Edge



Single code base across multiple architectures



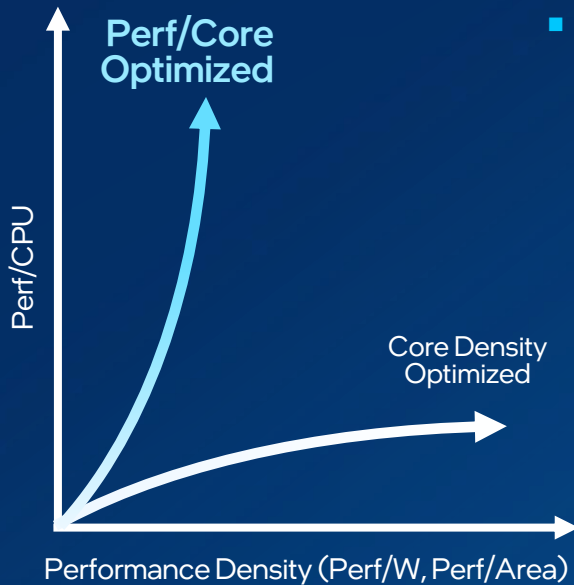
Data Center Infrastructure Requirements Evolving



- Different requirements driving \$TCO
Perf/Core, Perf/Watt, Perf/VM, Perf/Socket
- Continued demand for high-core performance
- Growing demand for cores that deliver highest performance-per-watt

CPUs Optimized for Mainstream Compute

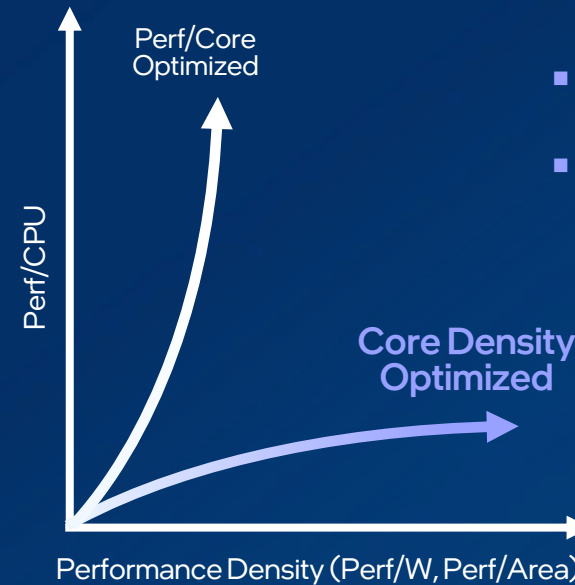
P-core



- High-core performance
- Workload-optimized performance with built-in accelerators

Optimized for Performance

E-core



- Performance-per-watt optimized
- High-core density
- High-throughput performance

Optimized for Efficiency

4th Gen Intel® Xeon® Arrives with Strong Customer Adoption

450+

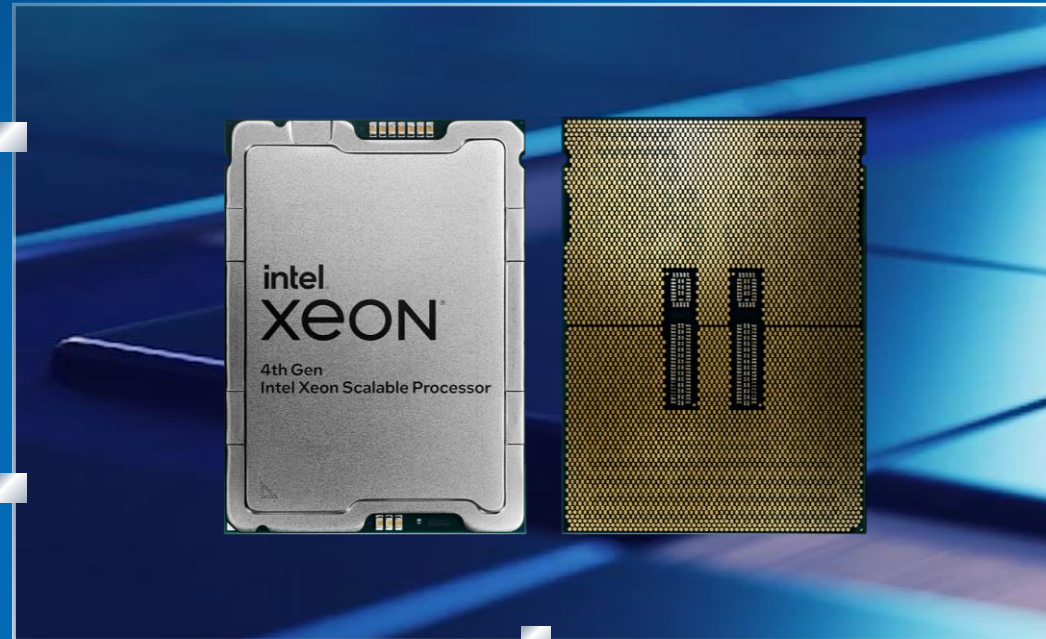
DESIGN WINS

The most ever for
any Xeon family

200+

DESIGNS SHIPPING TODAY

Most ever on embargo
lift/intended shipping day



50+

ALL MAJOR OXMS* SHIPPING

* Original equipment manufacturers +
original design manufacturers

Top 10

Global CSPs* deploying now
and throughout 2023

* Cloud service providers

Supply

Meeting customer demand today and healthy throughout 2023



5th Gen Intel Xeon Scalable Processors

Formerly codenamed "Emerald Rapids"

Sampling today, on schedule to deliver in Q4 2023

High-quality silicon

Volume validation underway

Higher performance-per-watt in same power envelope

Increased gen-on-gen core density

Same platform as 4th Gen Xeon

Easy migration path, from previous generation



Intel® Xeon® Processors codenamed Granite Rapids

On schedule to deliver in 2024, closely following Sierra Forest

Excellent silicon health

Hitting all major engineering milestones

Performance optimized

First P-Core Xeon on Intel 3

Platform improvements

Increased core density, memory & I/O innovations



“As the market leader in this segment, our focus is on strategic adoption of new technologies that keep us ahead of the curve and in front of the competition.

The initial platform progress we are seeing with Intel’s Sierra Forest is fueling our confidence and invigorating that mission.”

Dave Lincoln

VP of Networking & Emerging Server Solutions



**Hewlett Packard
Enterprise**

“For decades, HPE and Intel have collaborated on engineering projects to usher in advanced performance and efficiency for a number of enterprise workloads. Combining our forces is what keeps our industry moving forward. We are pleased to continue that strong collaboration and help play a role in influencing the design and architecture of **Granite Rapids, Intel’s future-generation processor. We look forward to welcoming Intel’s upcoming innovation.**”

Krista Satterthwaite

Senior Vice President and General Manager,
Mainstream Compute, at HPE

Lenovo

“Leveraging Lenovo’s established in-house design and manufacturing strategy and Intel’s deep engineering capability, **the future platform based on Intel’s Granite Rapids processors booted in record time. This was one of the fastest and most efficient power-on implementations we have experienced** and we are excited to deliver this new emerging technology faster to further enable our customers’ digital transformations.”

Kamran Amini

Vice President and General Manager of Server & Storage, Lenovo Infrastructure Solutions Group

intel®

XEON®

Intel® Xeon® Processor codenamed Sierra Forest

First Xeon processor with Efficient-core (E-Core)

Sampling today, shipping 1st half of 2024

Excellent silicon health

Silicon power-on;
Operating systems booted
in <18 hours

Lead vehicle for Intel 3

144 processor cores

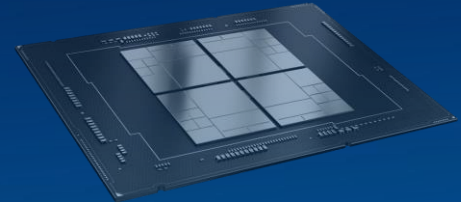
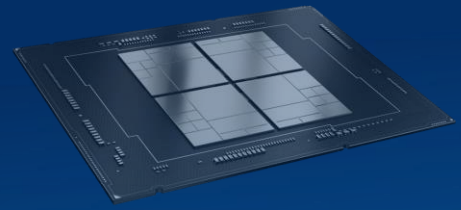
New class of Xeon

Built for cloud-optimized
workloads

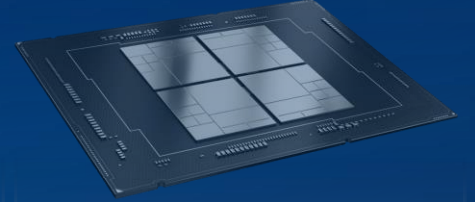
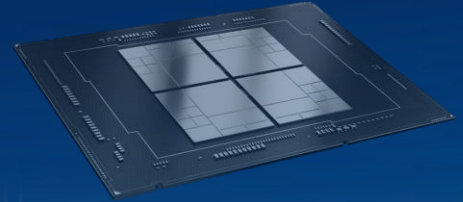


Executing on Our Xeon Roadmap

CPU P-Core



CPU E-Core



4th Gen Intel® Xeon® Scalable processors

5th Gen Intel® Xeon® codenamed Emerald Rapids

Next-Gen Intel® Xeon® codenamed Sierra Forest

Next-Gen Intel® Xeon® codenamed Granite Rapids

Next-Gen Intel® Xeon® codenamed Clearwater Forest

Today

Q4 2023

2024 (First Half)

2024 (closely following Sierra Forest)

2025



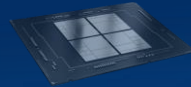
DCAI Architecture Evolution

CPU P-Core

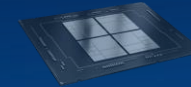


4th Gen Intel® Xeon® Scalable processors

Intel® Xeon® CPU Max Series

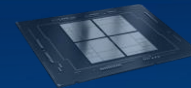


5th Gen Intel® Xeon®
codenamed Emerald Rapids



Intel® Xeon® Processors
codenamed Granite Rapids

CPU E-Core



Intel® Xeon® Processor
codenamed Sierra Forest



Intel® Xeon® Processor
codenamed Clearwater Forest

GPU



Intel® Data Center GPU Flex Series
codenamed Arctic Sound-M



Intel® Data Center GPU Max Series
codenamed Ponte Vecchio



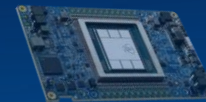
Intel® Data Center GPU Flex Series
codenamed Melville Sound

Next-Generation Accelerator
Architecture
Codename: Falcon Shores

Dedicated AI



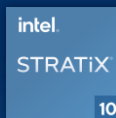
Habana®
Gaudi® 2



Habana®
Gaudi® 3

Next-Generation Accelerator
Architecture

FPGA



15 new FPGAs on
schedule to PRQ in 2023



Next Gen
FPGAs

Roadmap: 2023-2025

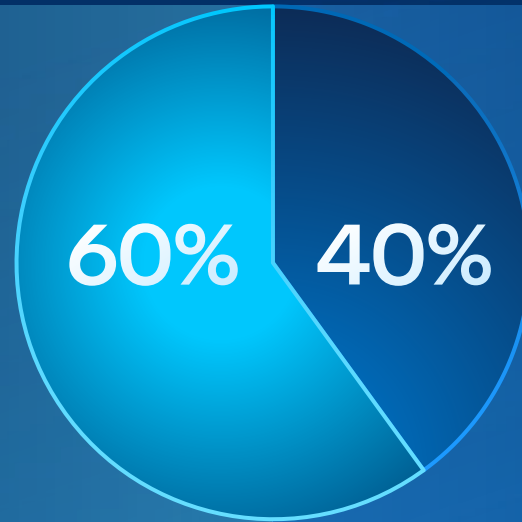
AI Accelerator Opportunity

>\$40B Logic Silicon TAM by 2027*

AI Silicon

General Compute

- Primarily managed by CPUs
- Processing, ingesting, management and movement of data
- Small- to medium sized AI models



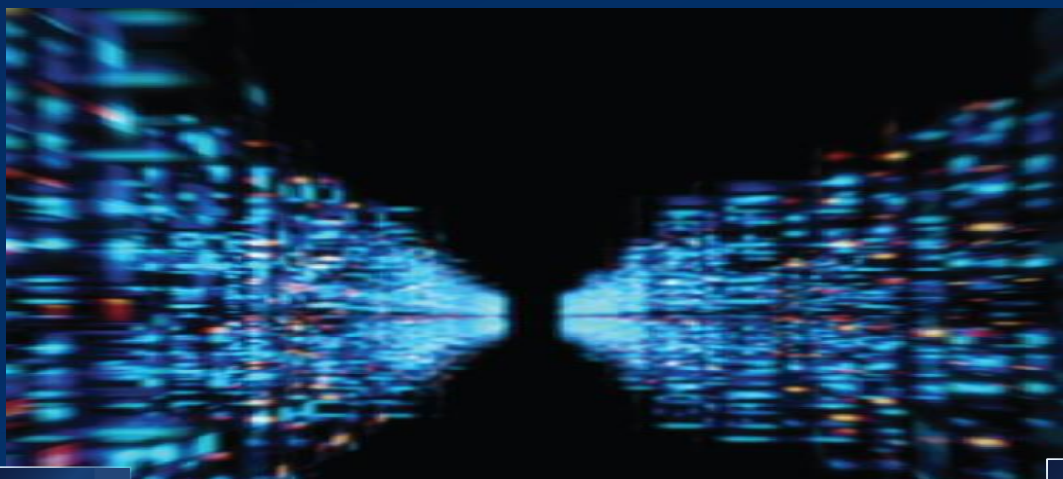
Accelerated Compute

- Serviced today by GPUs and special accelerators
- Large models (>100B parameters)

Demand for General Compute
and Accelerated Compute Growing with the Market

Using AI to Accelerate Internet Video

Video Processing



Build

Content Distribution



Deploy

Scale



Statistical AI analysis using AVX-512 and Intel® DL Boost to accelerate the video processing pipeline



Accelerated & encrypted content for distribution using Intel DSA and Intel QAT

AVX = Advanced Vector Extensions, DLBoost = Deep Learning Boost, DSA = Data Streaming Accelerator, QAT = Quick Assist Technology



Hugging Face

“We recently presented a benchmark using Habana Gaudi2 and the Hugging Face Transformers library that **enables you to run inference faster than with any GPU currently available on the market.**”

Jeff Boudier
Product Director, Hugging Face

stability.ai

“Intel has enabled stable diffusion models to run efficiently on their heterogeneous offerings from Intel 4th Gen Xeon Scalable Sapphire Rapids CPUs to accelerators like Gaudi and hence is a great partner to democratize AI. We look forward to collaborating with them on our next generation language, video and code models and beyond.”

Emad Mostaque
Founder and CEO, Stability AI

Scaling AI Compute

From the cloud, to the network, to the edge

Large-scale data center cluster

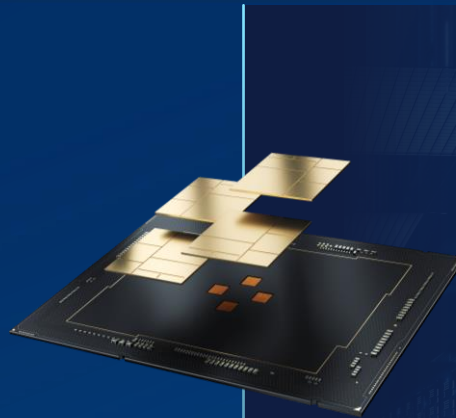
- Hundreds of billions of parameters models
- 256 Xeon processors
- 512 Gaudi deep learning accelerators

System-level approach

- Networking
- Memory bandwidth & capacity
- Software supporting industry frameworks

Portable models with Intel OpenVINO

- Build once, deploy anywhere
- Millions of downloads, hundreds of thousands of developers
- Used across a broad range of verticals



97%

Scale Efficiency

Democratizing AI

with software

Greg Lavender

Senior Vice President, CTO

General Manager, Software and Advanced Technology Group



intel.

Democratizing AI for Everyone



Open

Programmability



Choice

Compatibility



Trust

Inference at the Edge



Scaled

Delivery Mechanism
Infrastructure

Open Accelerated Computing for AI

Hardware / Architecture

Open = Ecosystem Adoption

Open
Programmability

 PyTorch

 TensorFlow

 DeepSpeed

 Transformers

SOURCES

<https://github.com/pytorch/pytorch/pulse>

<https://www.intel.com/content/www/us/en/developer/articles/technical/pytorch-2-0-new-performance-features-for-ai.html>

<https://www.businesswire.com/news/home/20220524005460/en/Intel-oneDNN-AI-Optimizations-Enabled-as-Default-in-TensorFlow>

Open = Programmability

Open
Programmability

SYCL™

Choice = Open Accelerated Computing

Choice
Compatibility

1[™]
oneAPI

over 85%
Increase in Install Base '21-'22

SOURCE: Internal Intel measurement based on telemetry from our software installers.

Choice = Open Accelerated Computing

Choice
Compatibility

1
oneAPI

OpenVINO™



6.2 million
Intel active developers

64%
of AI/ML developers using Intel tools

SOURCE: Q4 2022 Intel Active Developers Survey, Slashdata, Global 2023. Developer population estimates from sources: IDC, Slashdata, and Evans Data Corporation

Choice = Compatibility

Choice
Compatibility

SYCLomatic

Nvidia CUDA

Migrate

C++ with
SYCL

Build

Deploy

~90%

CUDA Code Migrated Automatically to SYCL

SOURCE: Intel estimates as of September 2021. Based on measurements on a set of 70 HPC benchmarks and samples, with examples like Rodinia, SHOC, PENNANT. Results may vary.

Trust = Security at the Edge



Trust

Inference at the Edge

**Open Federated
Learning**
(OpenFL)

SOURCE: <https://www.intel.com/content/www/us/en/newsroom/news/vision-2022-news-overview.html>

Scale = Intel® Developer Cloud

Scaled

Delivery Mechanism
Infrastructure

cloud.intel.com



Democratizing AI for Everyone



Open

Programmability



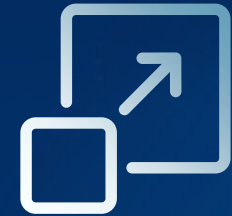
Choice

Compatibility



Trust

Inference at the Edge



Scaled

Delivery Mechanism
Infrastructure

Open Accelerated Computing for AI

Hardware / Architecture



In Summary

Competing in a **large and growing TAM**

Our roadmap is on track and we're hitting key milestones

Deploying assets to **truly democratize AI**

intel®

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Performance Disclaimer: Intel Max Series GPUs deliver up to 50% better performance for physics applications versus competitive products.

Configurations:

- Testing as of 1/31/2023 Intel Platform: 1-node 1x Intel® Xeon® 8360Y, HT On, Turbo Enabled, total memory 256GB DDR4-3200, 1x Intel® Data Center GPU Max 1550, Ubuntu 20.04, Kernel 5.15, oneAPI icpx Nightly 20230109
- Testing as of 1/18/2023 Competing Platform: 1-node 1x Intel® Xeon® 8360Y, HT On, Turbo Enabled, total memory 128GB DDR4-3200, 1x PCIe NVIDIA H100, Ubuntu 20.04, Kernel 5.15, GPU Driver 525.60.13, Intel LLVM 20230109, CUDA 12.0
- Workload: Alfvén Wave for grid sizes: 36^3 , 48^3 , 72^3 , 96^3 , 132^3 , 192^3 , 264^3 , 390^3 , and 516^3 cells. DPEcho GitHub: <https://github.com/LRZ-BADW/DPEcho>