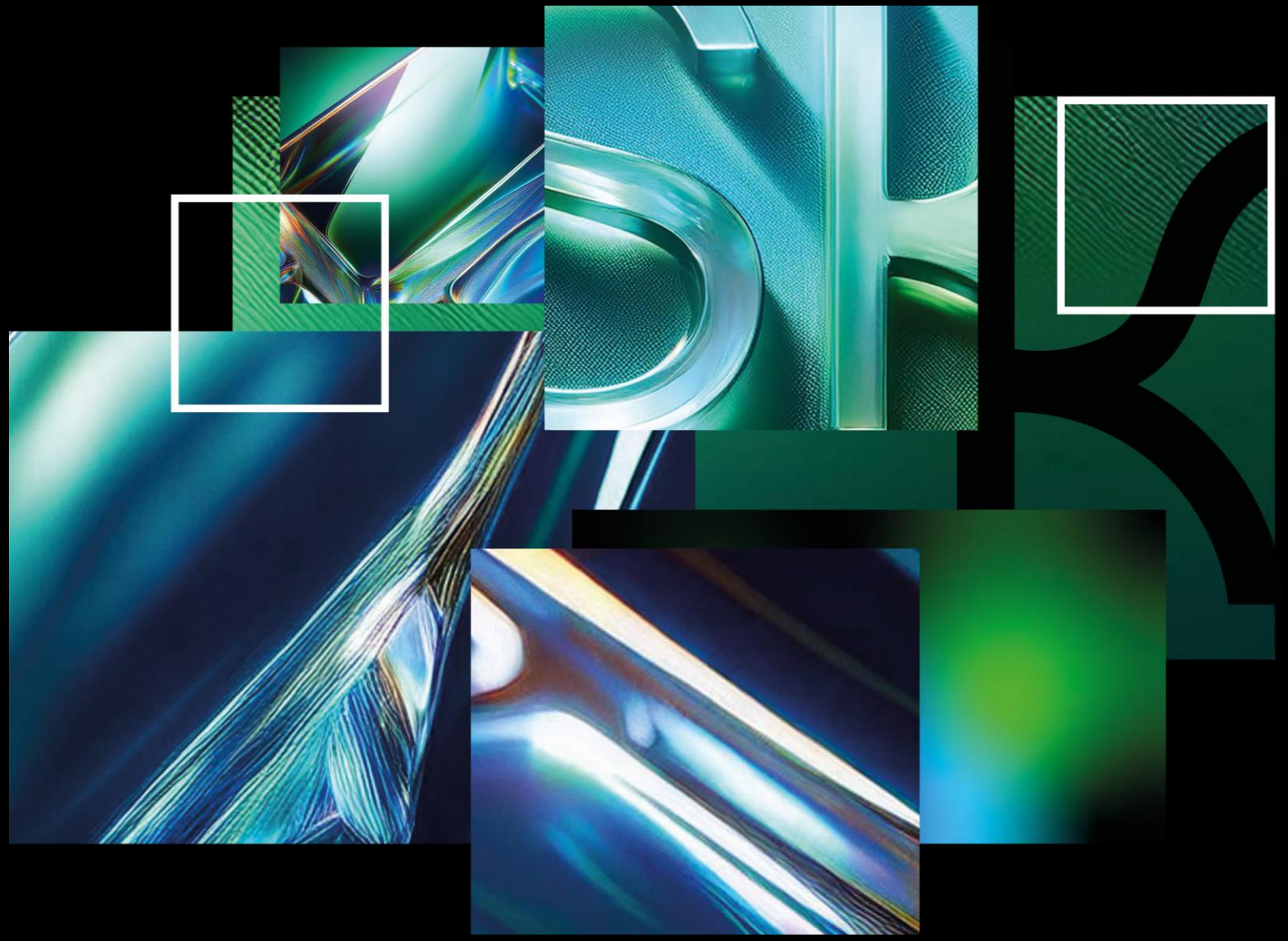
MicroLED Displays Fabricated Chip-First

Enabled by Low-Temperature Organic Transistor Technology



Smartkem

NASDAQ: SMTK

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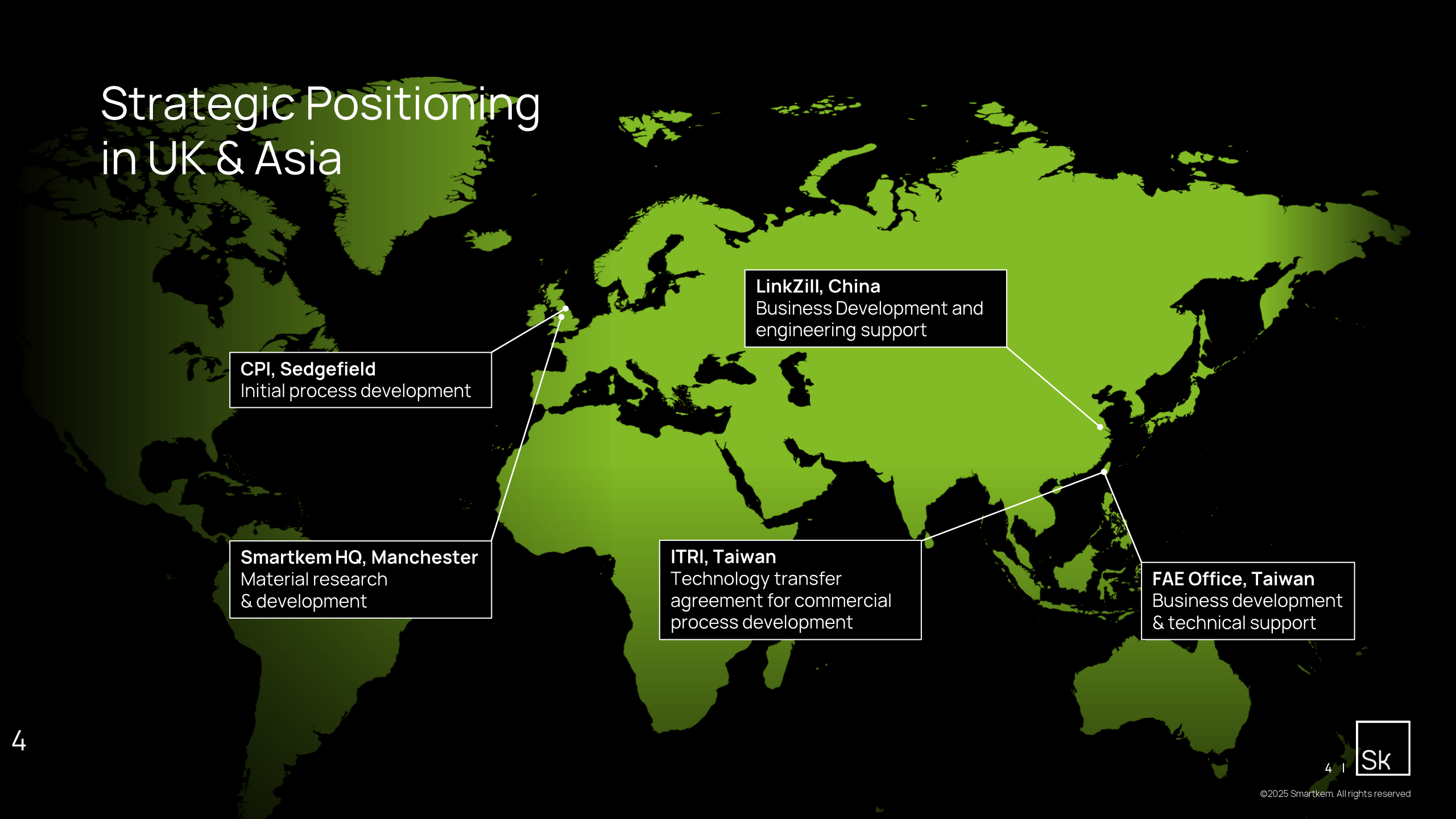
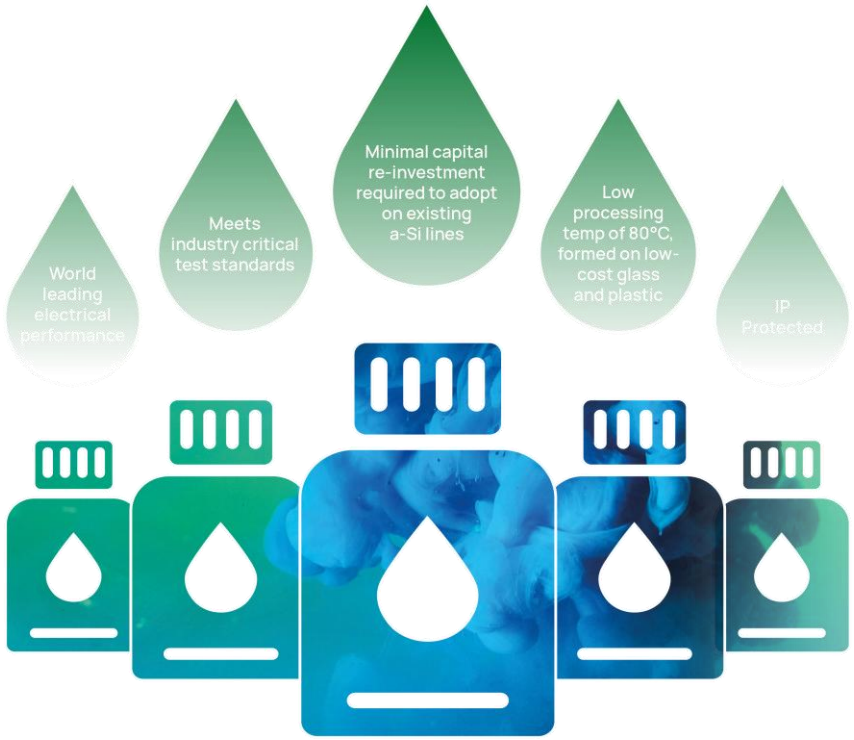
These statements may be identified by the use of forward-looking expressions, including, but not limited to, "expect," "anticipate," "believe," "estimate," "potential," "predict," "project," "should," "would," and similar expressions and the negatives of those terms. These statements relate to future events or our financial performance and involve known and unknown risks, uncertainties, and other factors which may cause actual results, performance or achievements to be materially different from any future results, performance or achievements expressed or implied by the forward-looking statements. Such factors include those set forth in the Company's filings with the Securities and Exchange Commission. Prospective investors are cautioned not to place undue reliance on such forward-looking statements, which speak only as of the date of this presentation. The Company undertakes no obligation to publicly update any forward-looking statement, whether as a result of new information, future events or otherwise.

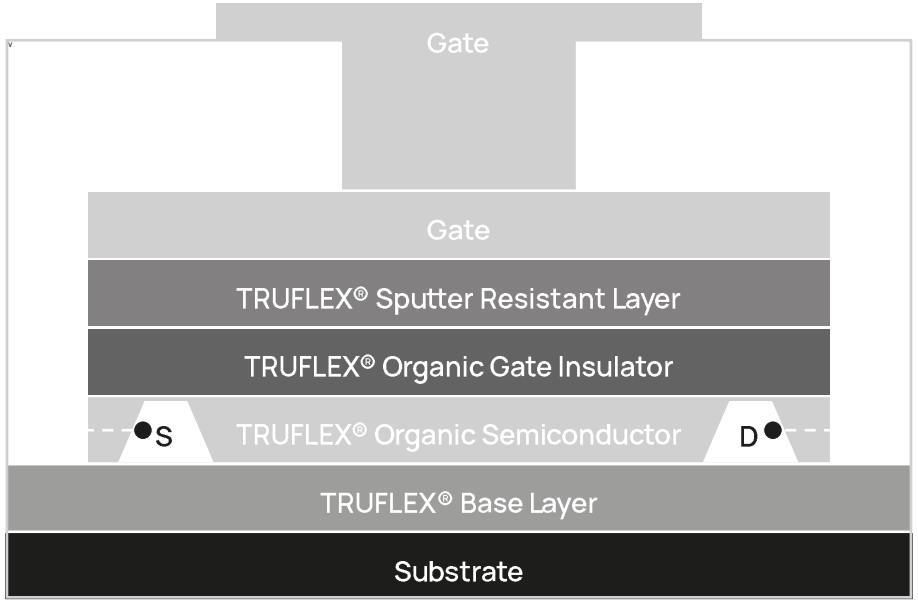
Smartkem (Nasdaq: SMTK) makes a new class of transistor using its proprietary advanced semiconductor materials.

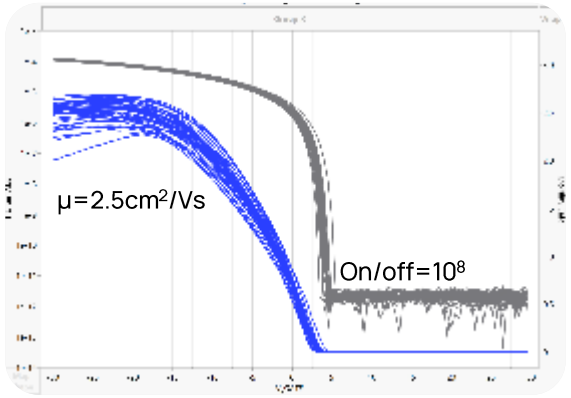
Strategic Positioning in UK & Asia

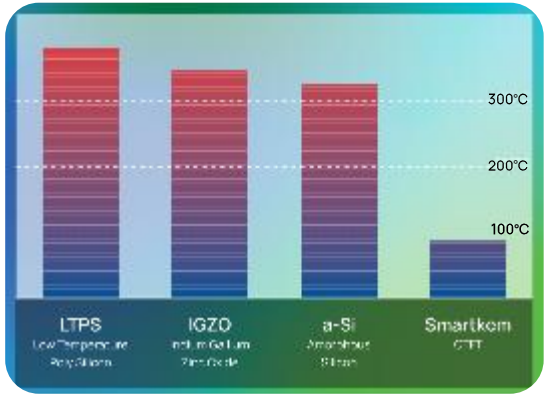


Smartkem's TRUFLEX® Materials









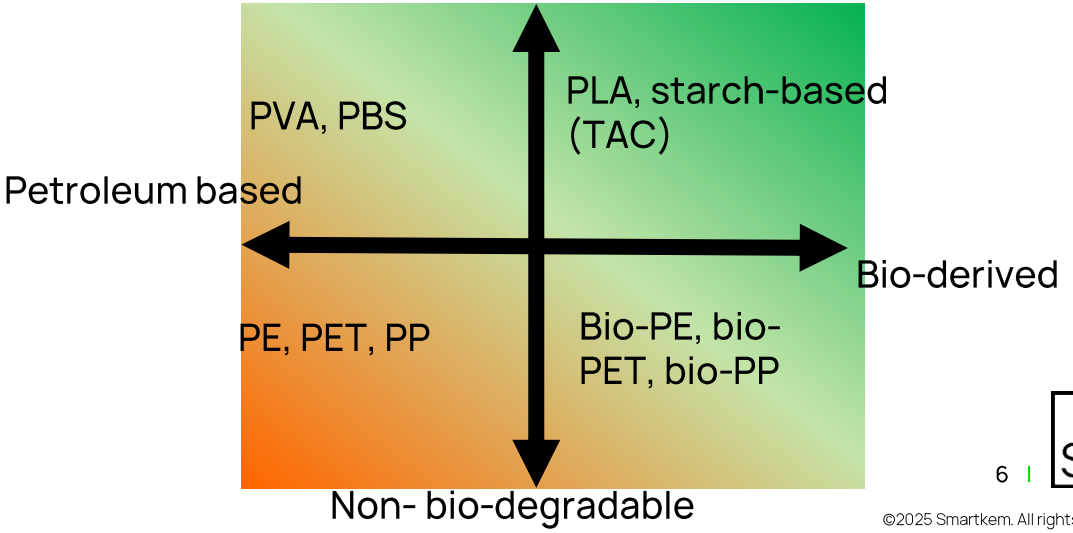
Benefits of low temperature TFT process

1. Energy use - Overall lower energy use in manufacturing (no PECVD)

2. Substrate type - wider choice of plastics with improved properties
   1. Transparency
   2. Biodegradability (<12 months)
   3. Bio-derived (e.g. cellulose)
   4. Low-cost

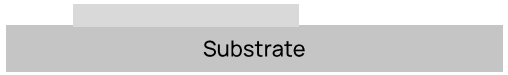
3. Integration benefits - TFT backplane could be processed on top of the device (OLED, micro-LED, etc), potential for R2R manufacturing

Plastic electronics should not add to the plastic waste problem



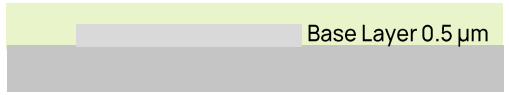
TRUFLEX® Stack – Dual Gate OTFT Process

Sputter and pattern back-gate metal by photolithography and wet etching

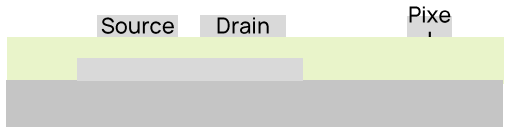


BG – Mask 1

Base layer spin coating and UV/thermal curing

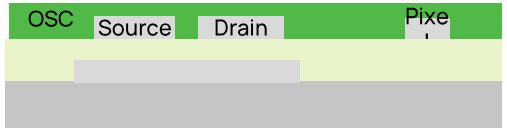


Sputter and pattern SD (50nm) by photolithography and wet etching

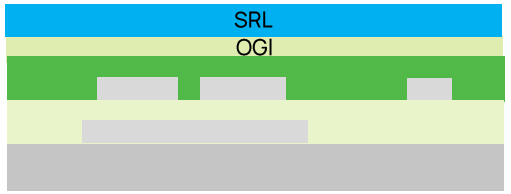


SD – Mask 2

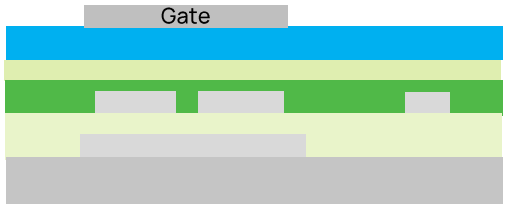
SAM and OSC spin coating and baking



OGI spin coating and baking, SRL spin coating and UV/thermal curing



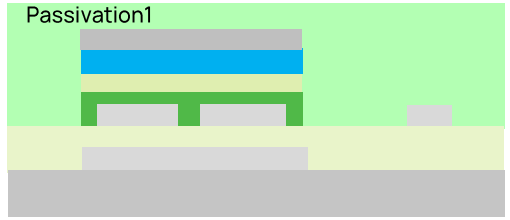
Sputter and pattern gate by photolithography and wet etching



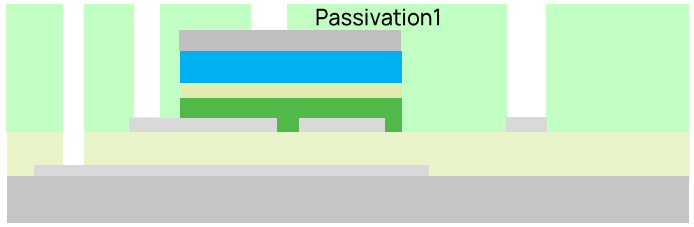
GM– Mask 3

RIE etching (O2/Ar)

Passivation layer spin coating and UV/thermal curing

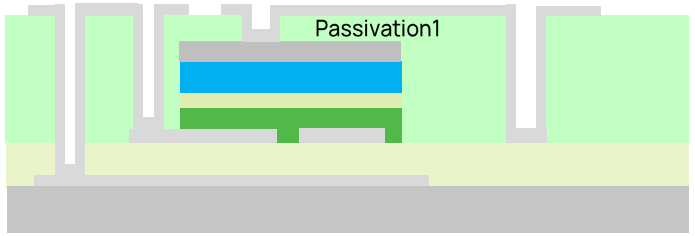


Passivation layer patterning using photoresist with dry etch transfer of pattern



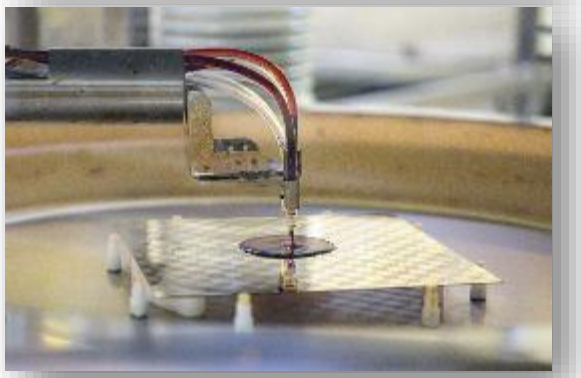
PV1 – Mask 4

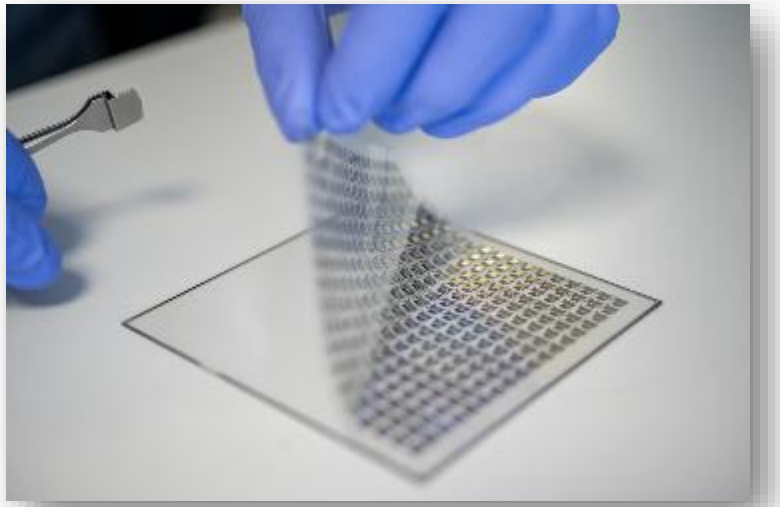
Sputter and pattern (50nm) gate contact metal by photolithography and wet etching

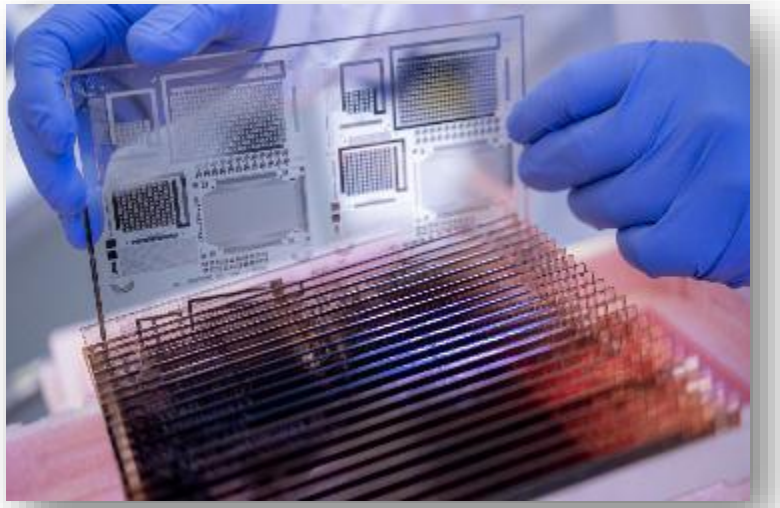


GC1 – Mask 5

OTFT fabrication equipment in UK for 4”,8”, 12” glass and flex

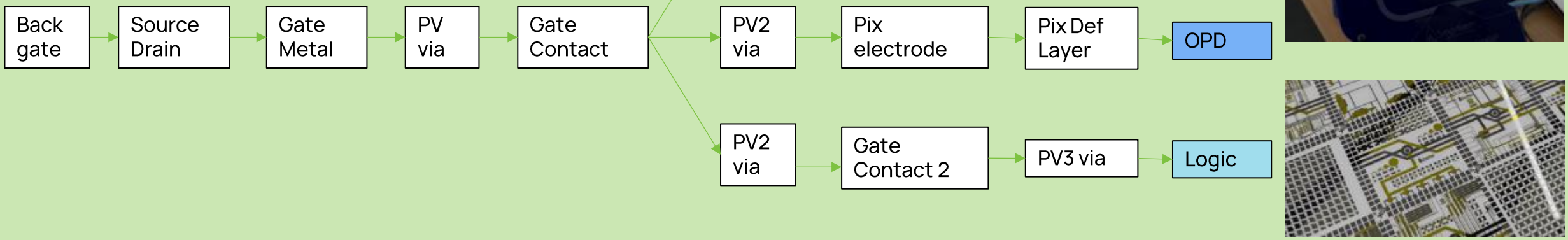




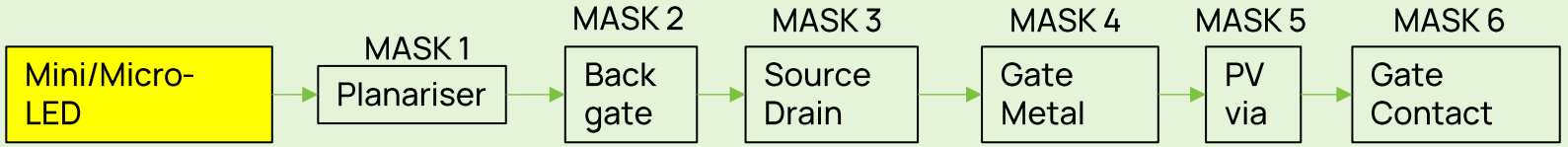


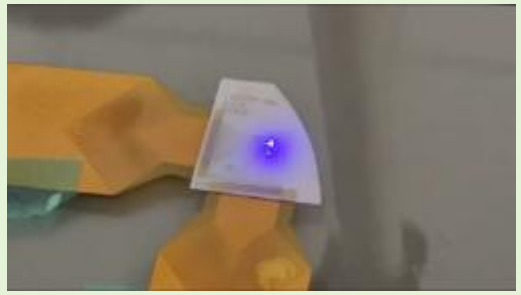
- Digital lithography – 1.5um minimum feature size
- 0.5um overlay accuracy

Process flow for OTFT Displays and Circuits



200ppi QVGA AMOLED





254ppi 48x48 OTFT-uLED (0.27” diagonal)

- Logic cells require 5 masks for fabrication (similar process flow as for OLED, OPD, microLED)
- Additional layers PV2/GC2/etc can be used for integration of OLED, OPD, wiring layers
- Capability in OTFT circuitry has been developed in parallel with display activities
  - It is not yet fully enough characterised to offer as a commercial foundry service
  - Digital lithography capability makes OTFT circuitry a low-cost R&D activity

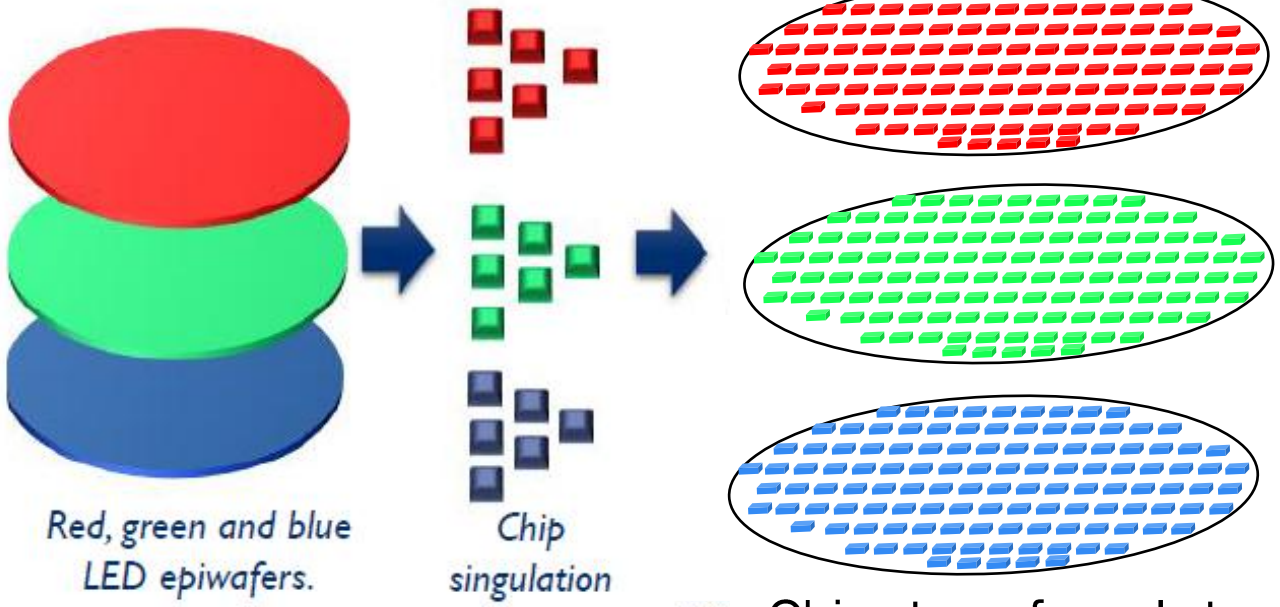
25ppi 27x48 OTFT-mini LED Backlight (2.17” diagonal)

MicroLED Display Benefits

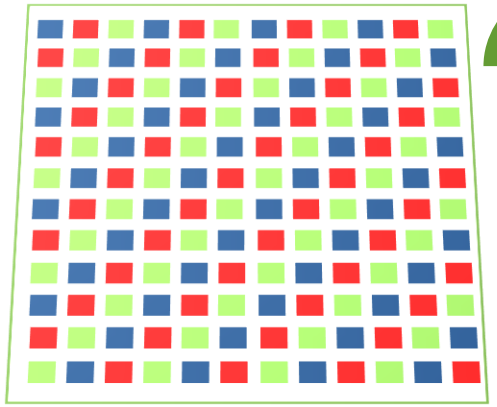
- Superior Brightness and Efficiency
- Longevity and Durability
- High Contrast and Colour Accuracy
- Scalability and Versatility
- Thinner and Lighter Designs

Mainstream Approach

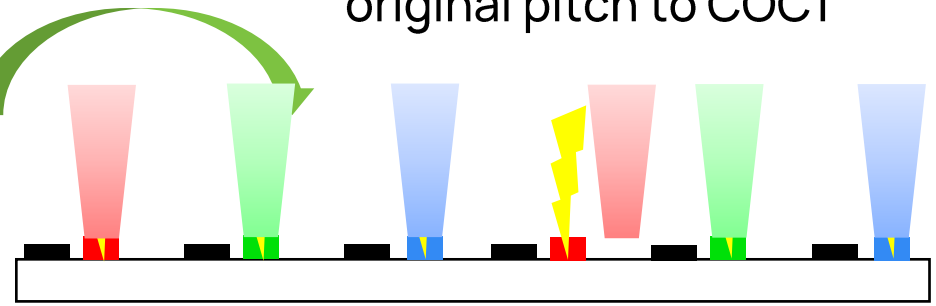
- Transfer 1 - from Sapphire substrate to Carrier 1 (COC1)
- Transfer 2 - from Carrier 1 to Carrier 2 (with pitch increase, sorting, and RGB)
- Transfer 3 -from Carrier 2 to backplane
- Weld/solder/bond the LEDs to the backplane
- Perform AOI and rework individual pixels which are distributed randomly across the array. The rework process is limited to one or two attempts and is not always successful. Laser re-work can potentially damage the TFTs in the backplane.



Chips transferred at original pitch to COC1

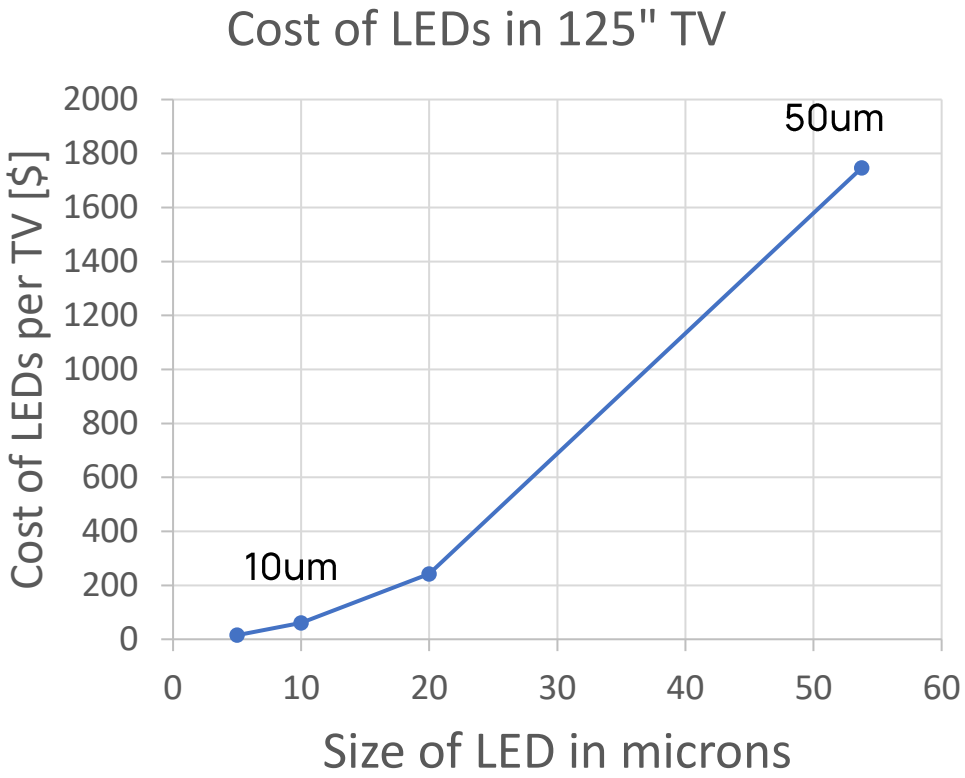


Chip sorting onto transfer sheet (COC2)

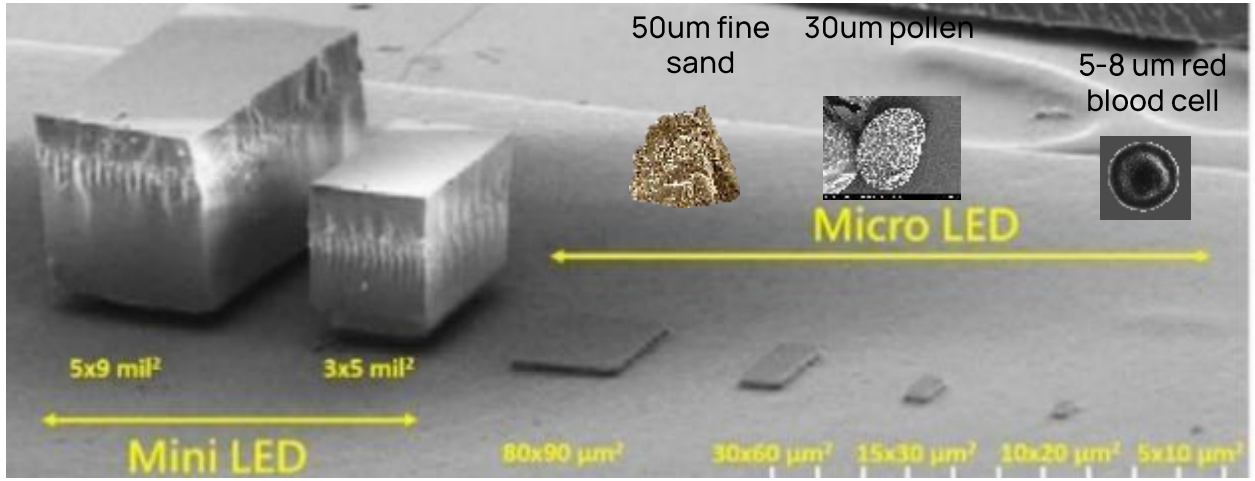


Transfer to TFT backplane – eutectic bond and test

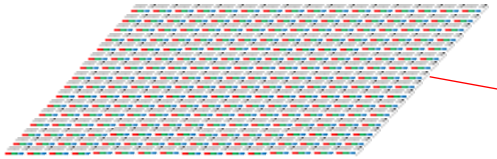
MicroLED needs small die sizes to be economical



- For micro-LED to be economical we need to be using <10 micron size LEDs for TV applications

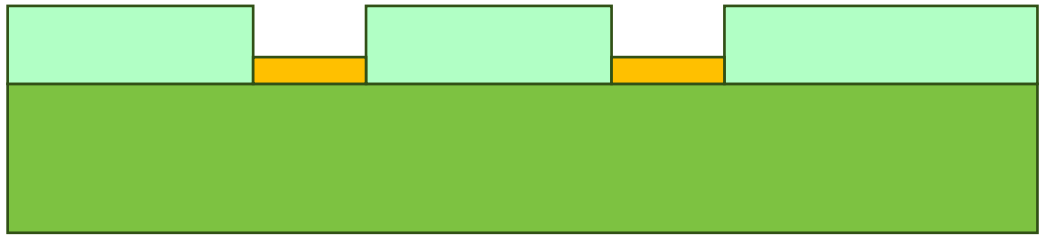


Challenge!
Arrange 24 million micro-LEDs smaller than grains of sand in the correct order and then solder them to make an electrical connection with >99.99999% yield

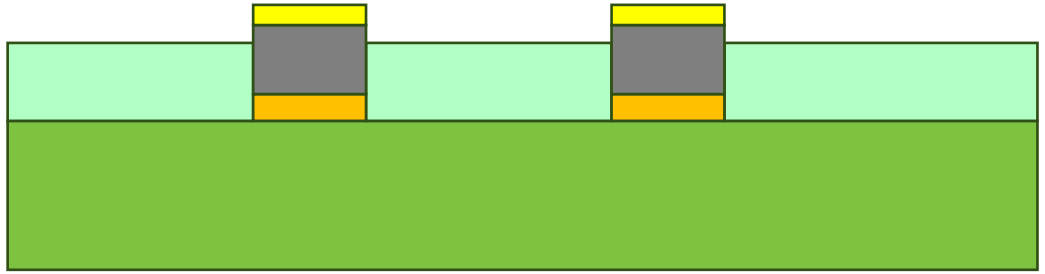


8 million pixels (xRGB)

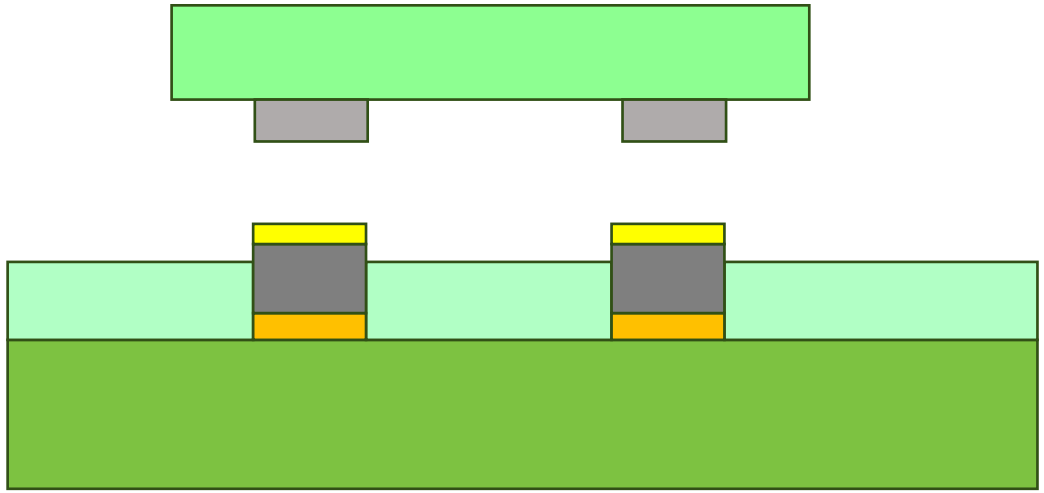
Eutectic bonding process – anode cathode pads on backplane (Cu)



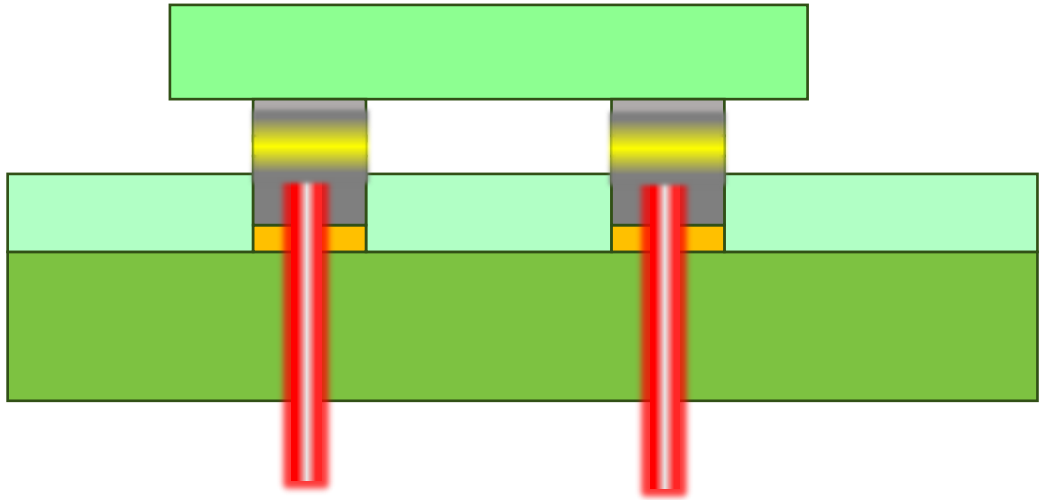
Eutectic bonding process – electroless nickel immersion gold (ENIG) bump



Eutectic bonding process – MicroLED placement

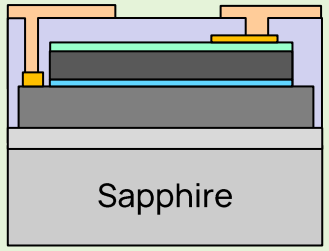


Eutectic bonding process – IR laser welding of pads to join metals

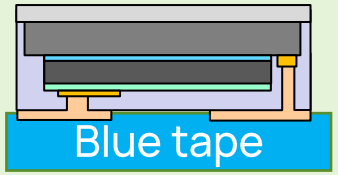


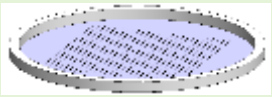
Chip-First µ-led Process – Monolithic Backplane Build on a COC2

a).

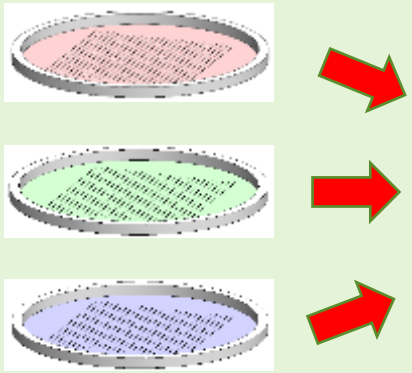


b). Laser lift-off onto blue tape

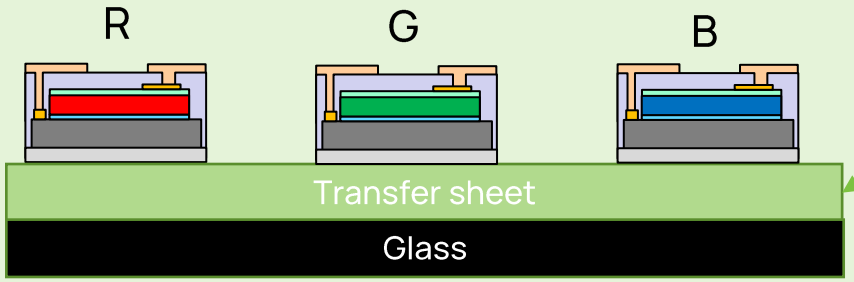




c).



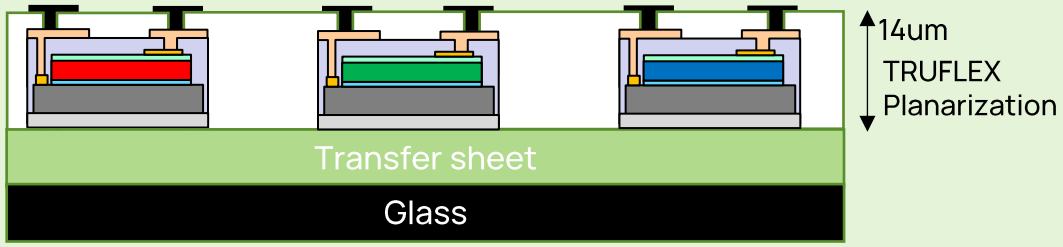
d). Laser-induced forward transfer (LIFT)
(pitch same as display)



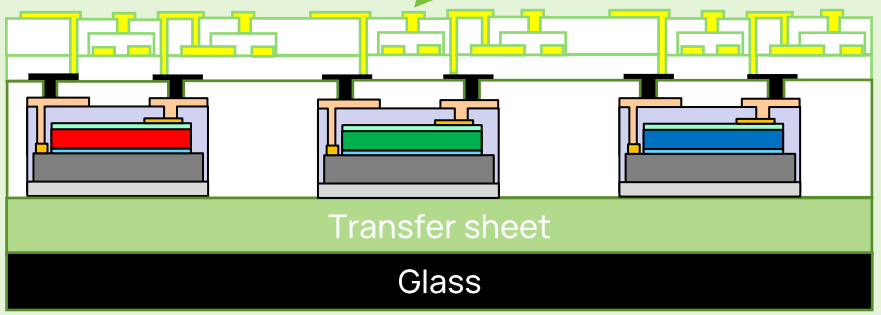
Chip on carrier 2 substrate (COC2)

Low temperature OTFT backplane processed on top of LEDs

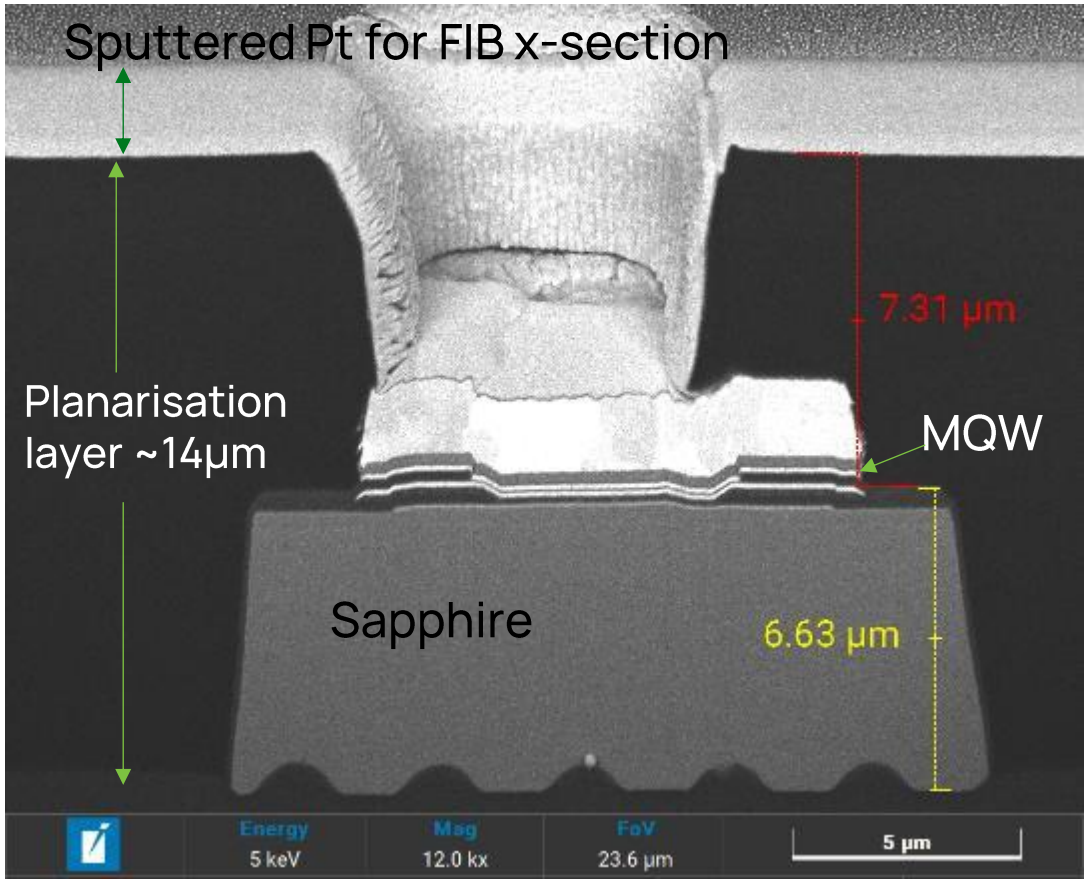
e). Planarize, etch vias and metallize contacts



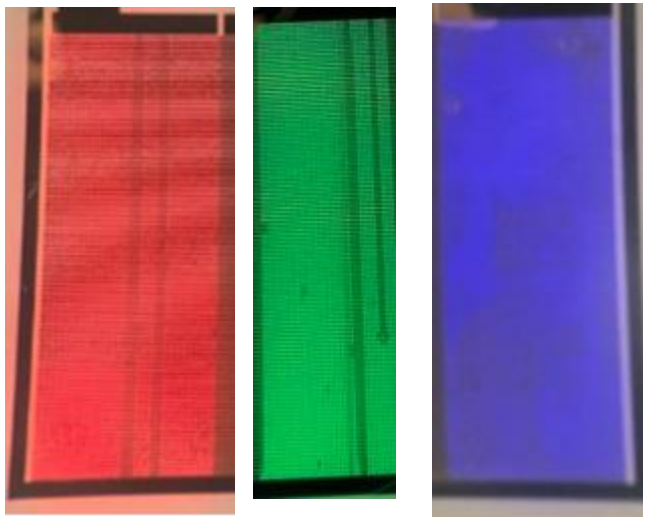
f).

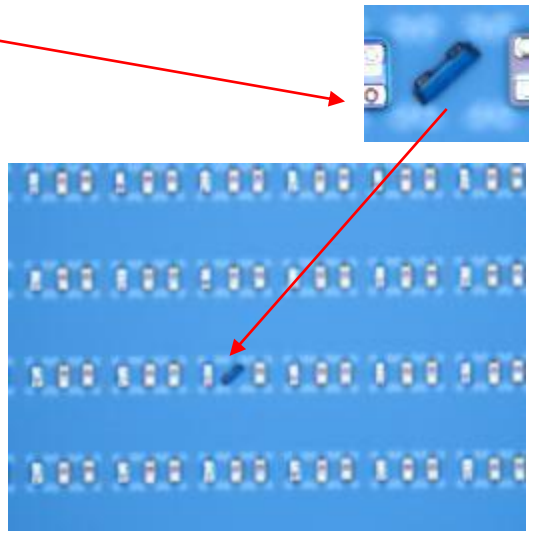


FIB x-section of via structure



- Verification of via clear-out through examination of x-section
- Positional accuracy ok (approximately +/-2um tolerance allowed on via position relative to the centre of the LED)
- Planarisation layer coats LED very well with little change in surface height at edges of device
- Yield is not yet perfect so more optimisation is required (may be related to occasional dies in the wrong place or die standing on end)





Chip-first and chip-last share several common processes

Chip first processing

Metal to metal via connection process

Low temperature TFT process (using OTFT only)

Processing overlap for both techniques

Laser lift-off or mechanical lift-off

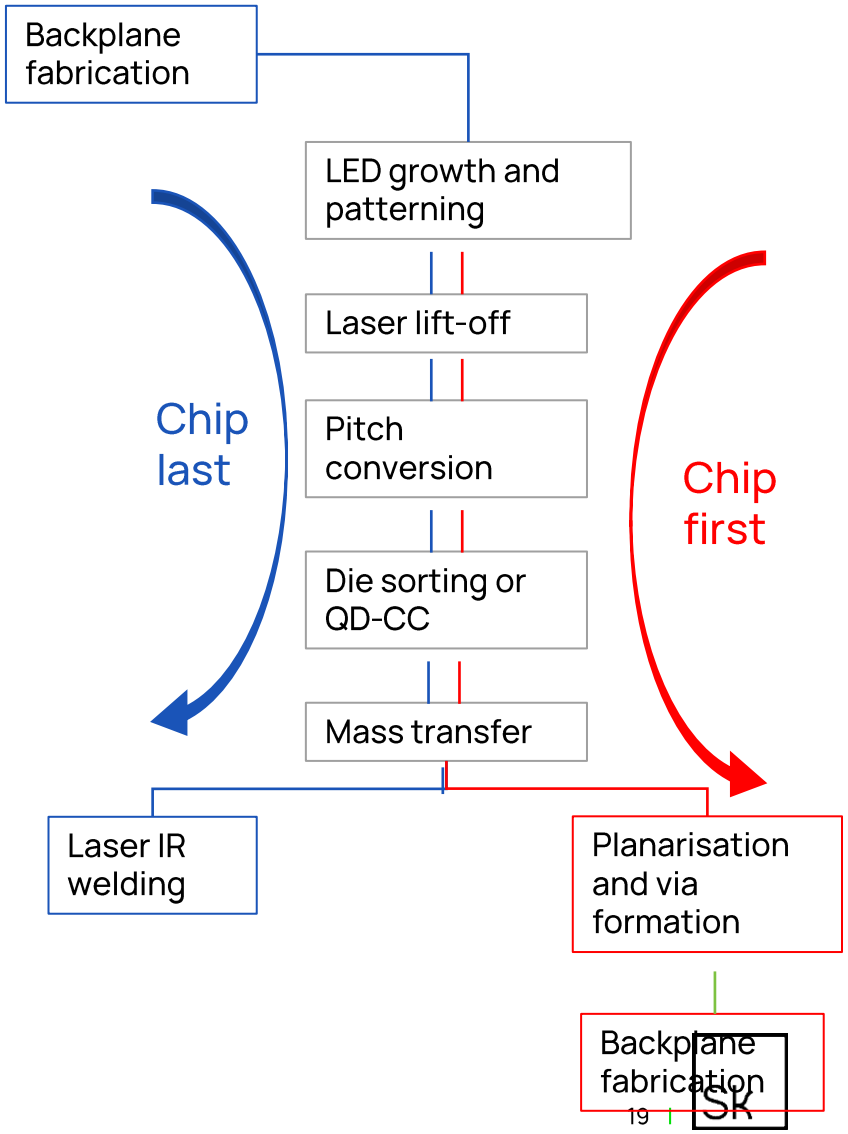
RGB die sorting or QD-colour conversion (QD-CC)

Pitch conversion using laser or stamp transfer

Chip-last processing

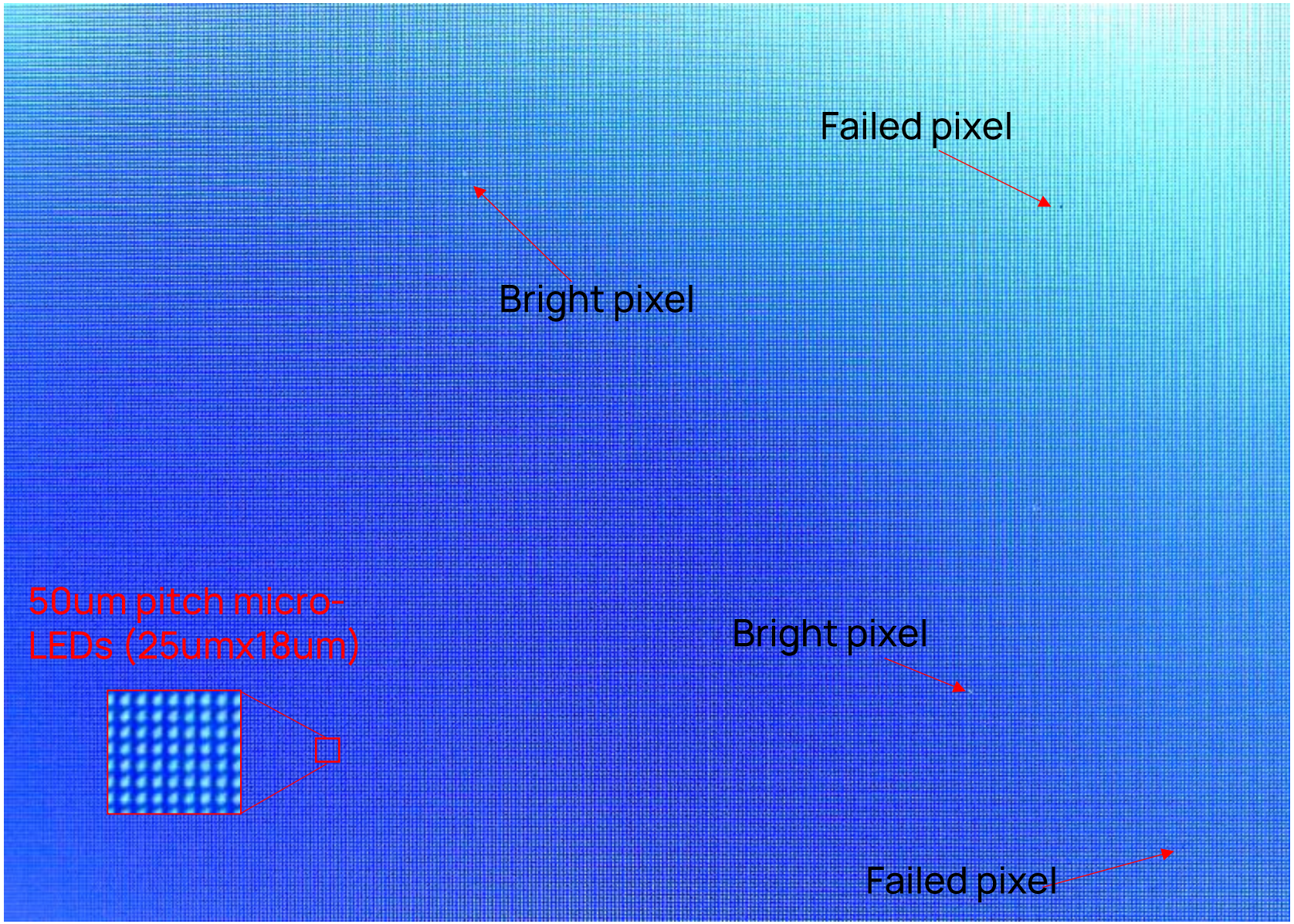
Eutectic laser bonding process

Backplane first (can be LTPS, oxide or OTFT)



Evaluation of yield of planarisation and via formation: 194K MicroLEDs

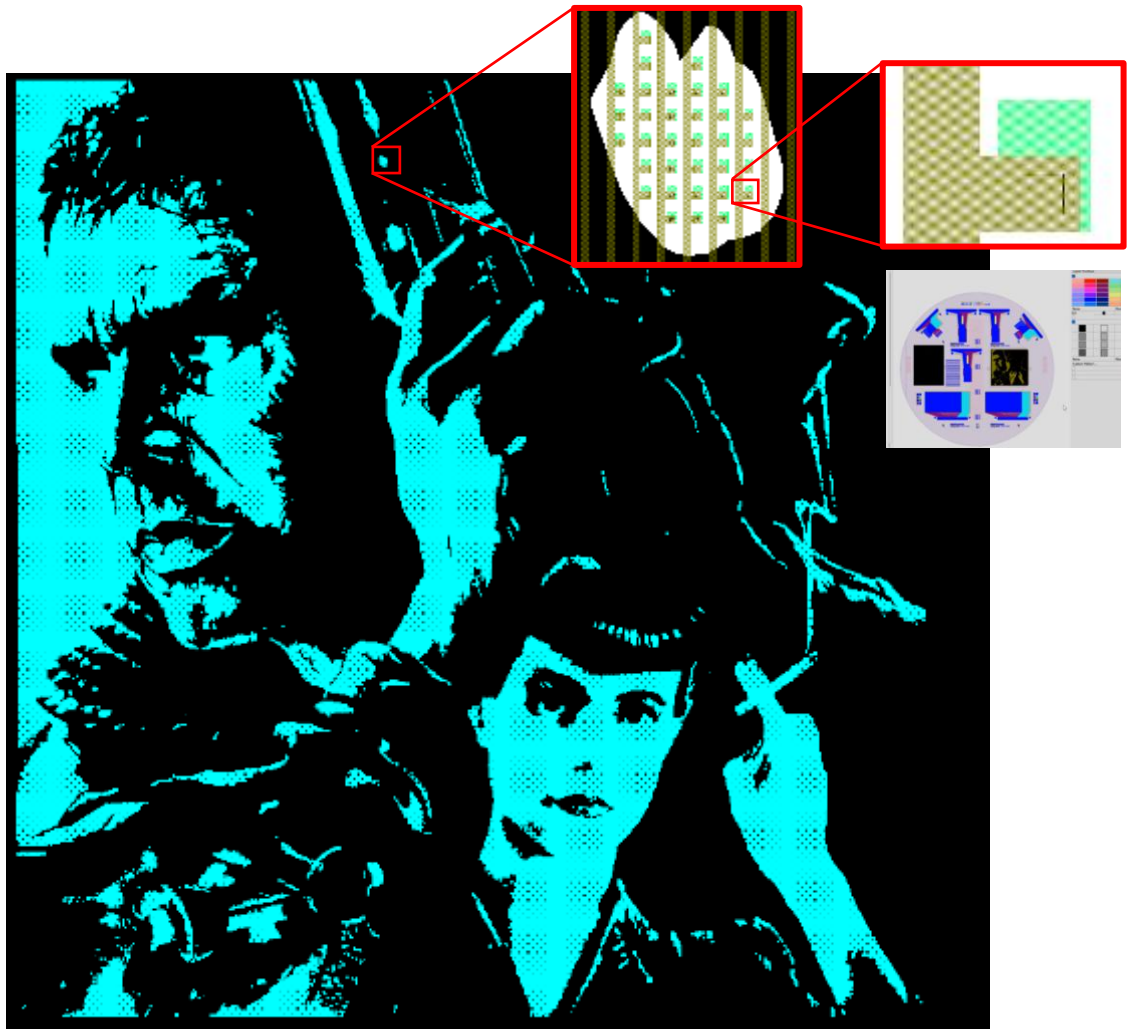
- Used sapphire wafer for the test as can ensure high yield and very accurate positioning of LEDs
- In the field of view of this image there are 194,000 micro LEDS of 25umx18um size wired up through a planarisation layer
- 2 bright pixels and 2 dark pixels are observed. This corresponds to a yield of 99.998%*
- Further improvements in yield are likely:
  - Change from the current contact mask aligner to stepper process for micro-LED production
  - Move from manual 4” substrate handling in class 1000 environment to automated handling in class 100 environment or better



* For a more accurate yield evaluation, further substrates require processing – this is only the result from one substrate

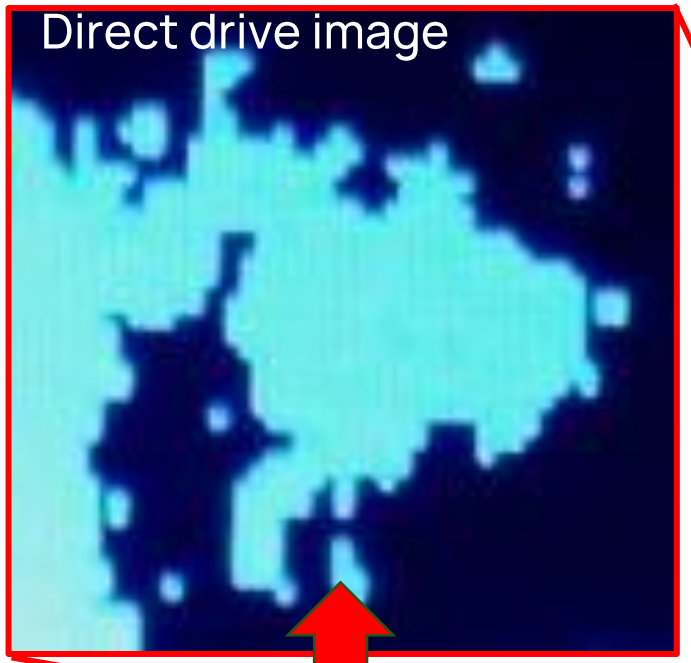
Upgrade of MicroLED production from contact to non-contact lithography (this time on Si wafer)

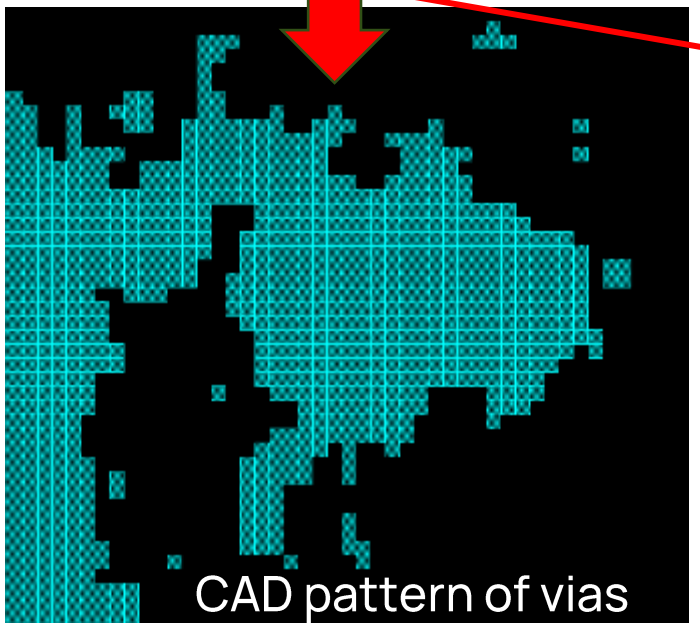
CAD pattern of vias and micro-LEDs

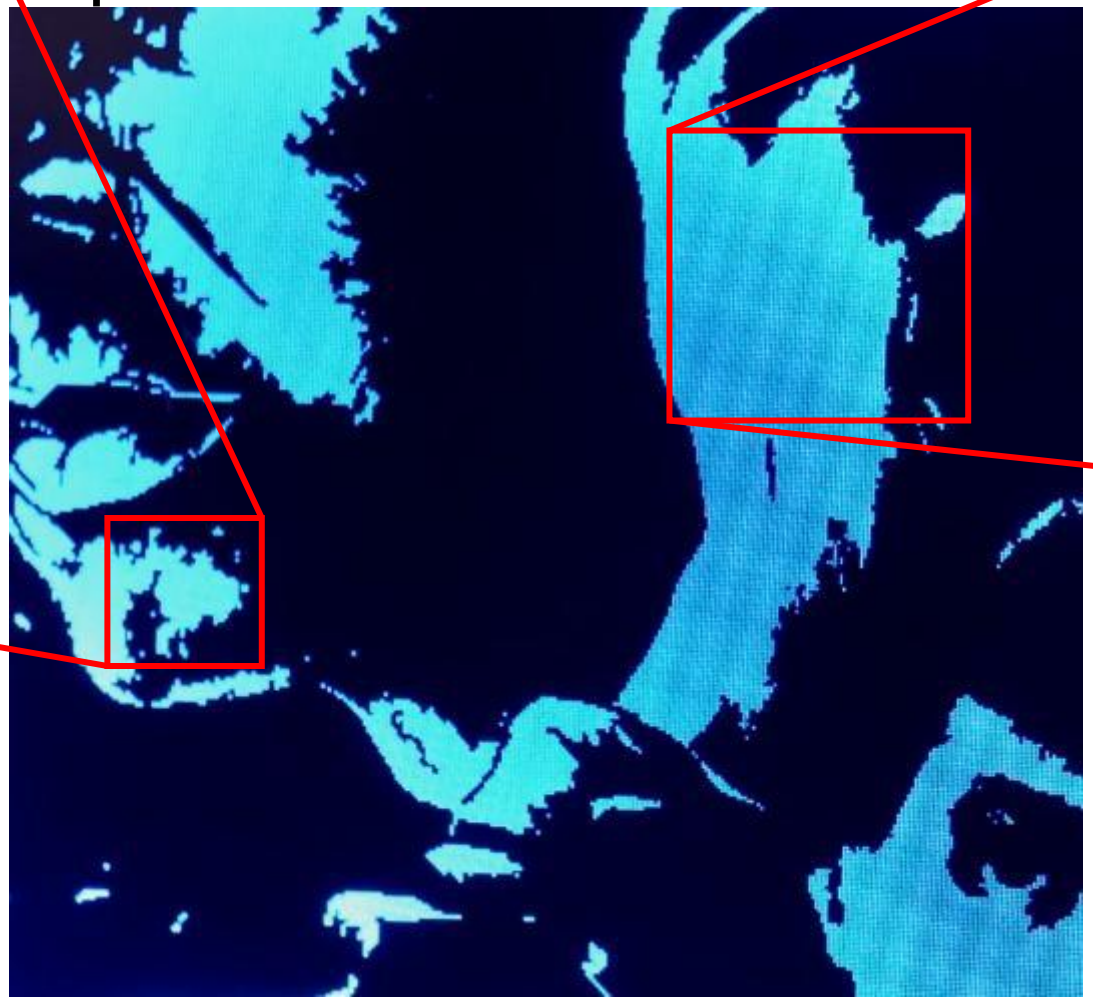


Direct drive image (110,000 lit micro-LEDs)

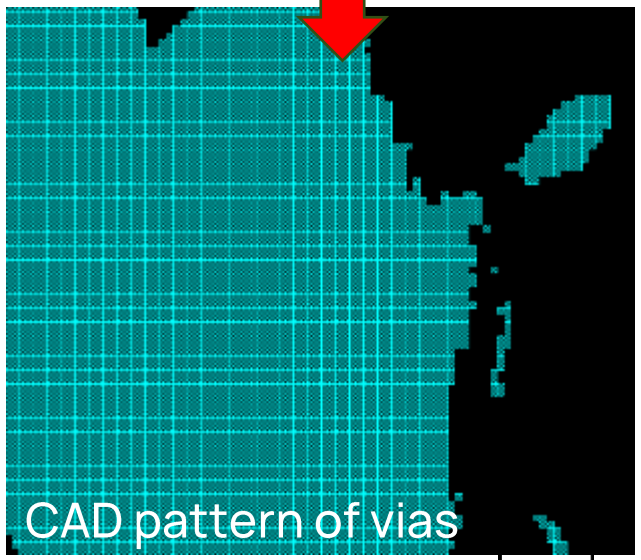
No defects or incorrect pixels found







Approximately 27000 micro-LEDs with no observed faults



Approximately 5000 micro-LEDs with no observed faults

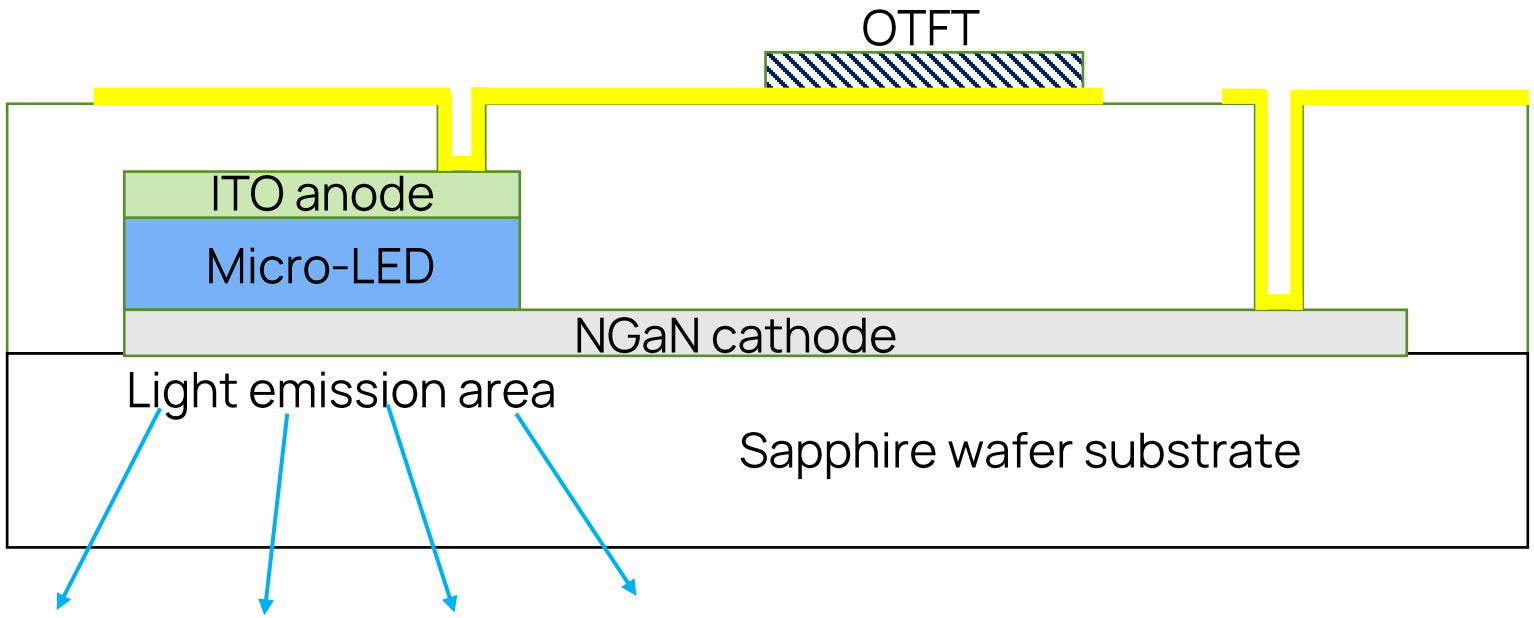
Exact match!

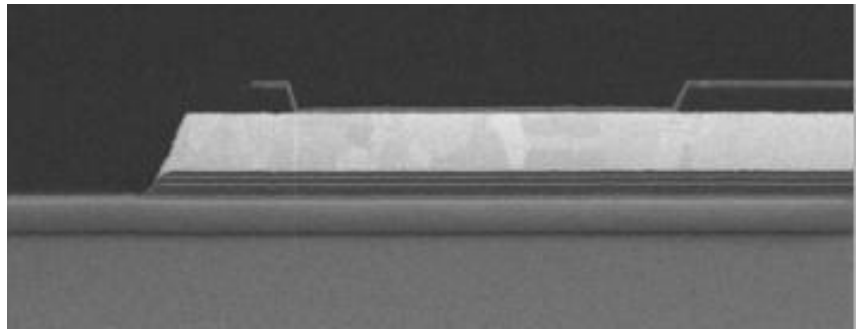
AM-OTFT micro-LED Monolithic Integration

Integrate OTFT backplane on top of micro-LED array on Sapphire or Silicon wafer (process temp < 150°C)

Monolithic integration means no transfer losses

Electrical connection will be reliable since it uses a via technology (already proven in TFT manufacturing with very high yield)



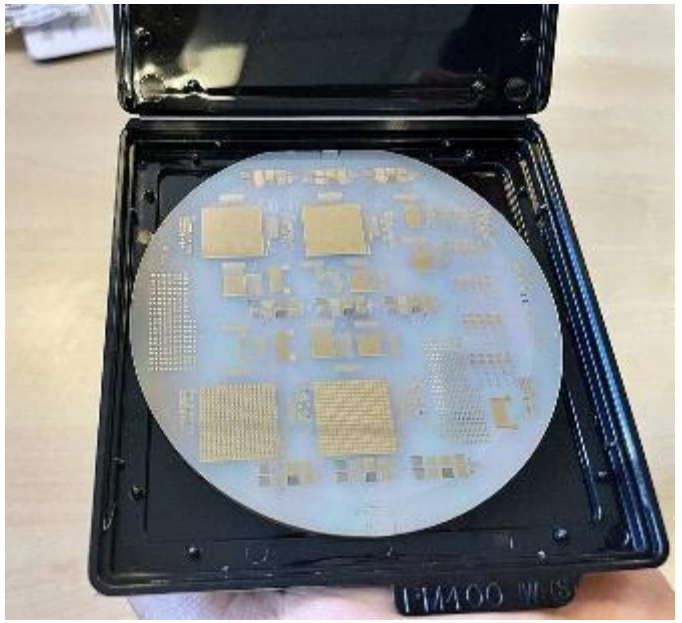


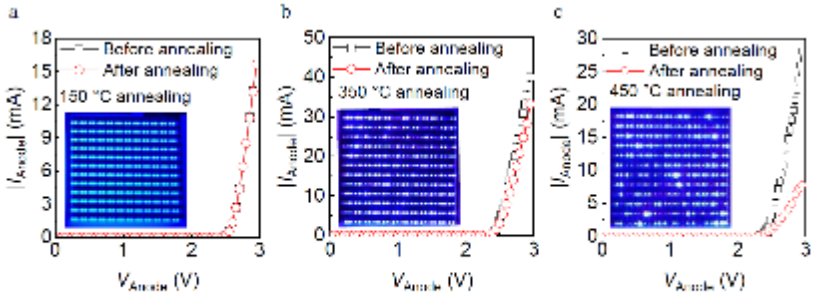
nature communications

Wafer-scale organic-on-III-V monolithic heterogeneous integration for active-matrix micro-LED displays

https://www.nature.com/articles/s41467-023-42443-8

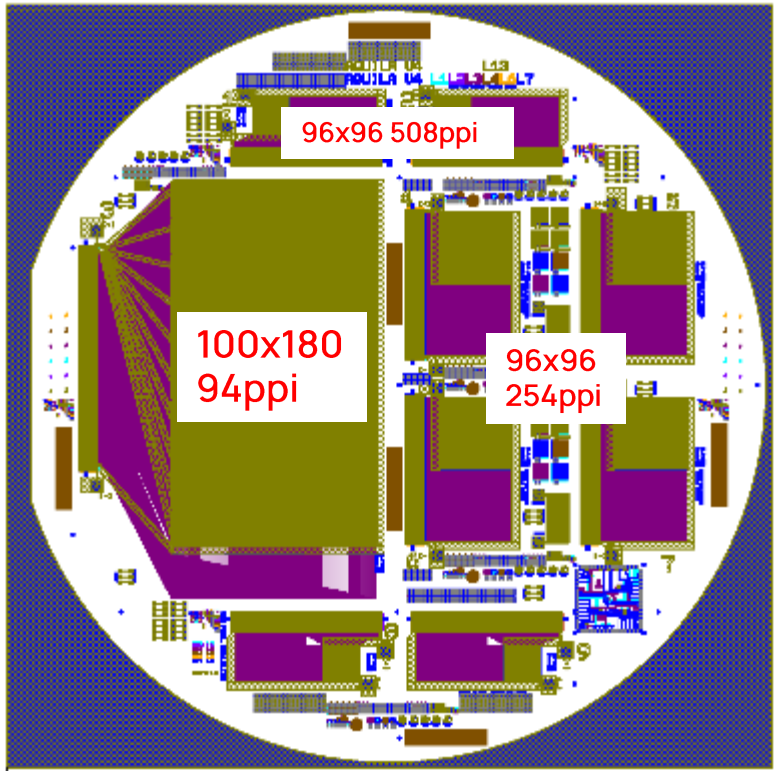
In collaboration with SJTU





Supplementary Fig. 3 Characterization of the micro-LED performance before and after annealing under different temperature: (a) 150 °C. (b) 350 °C. (c) 450 °C.

Monolithic MicroLED Design

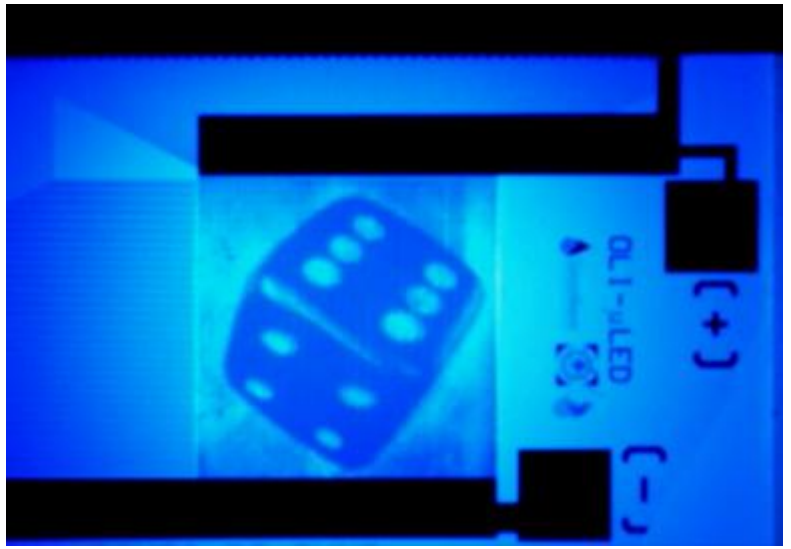


LinkZill

- 100x180 driver system (video rate)
- Capable of 60xRGBx100 colour
- Compatible with OTFT based gate-on-array

100 x 180 - 94ppi (some defects)

96x96 - 508ppi (no visible defects)

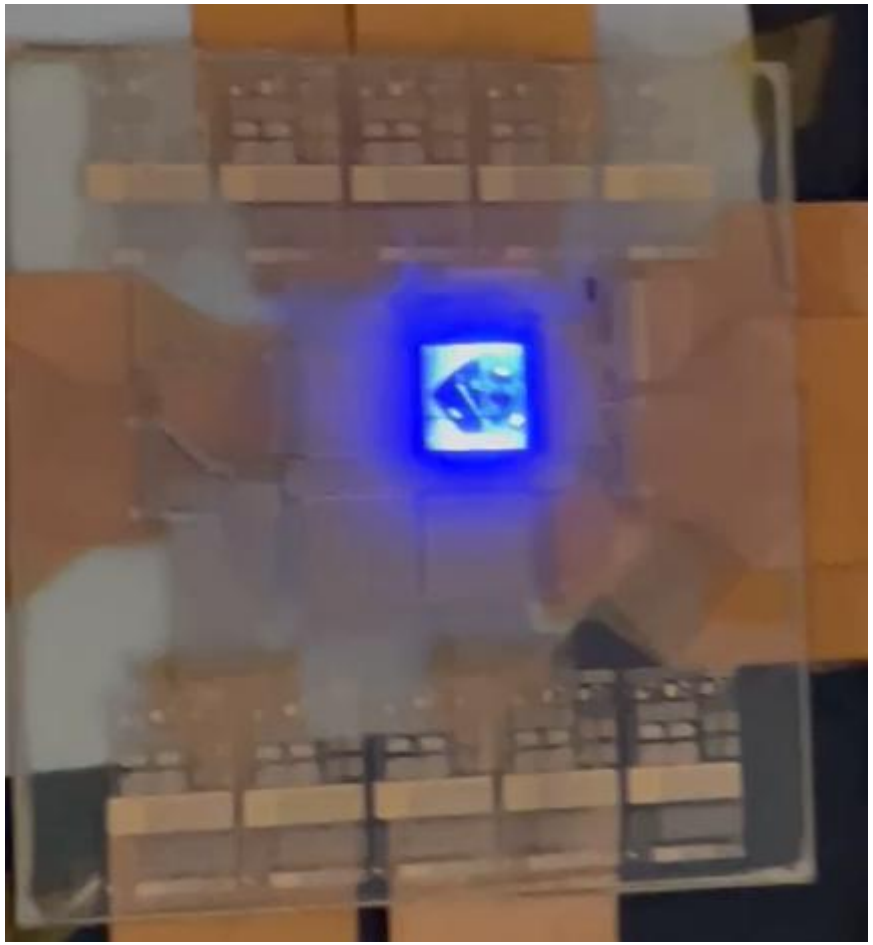


An Introduction to the Monolithic OTFT-on-µLED Process

Exploiting Smartkem's Ultra-Low Process Temperature to unlock novel methods of microLED backplane manufacturing

Smartkem

Chip-first MicroLED display

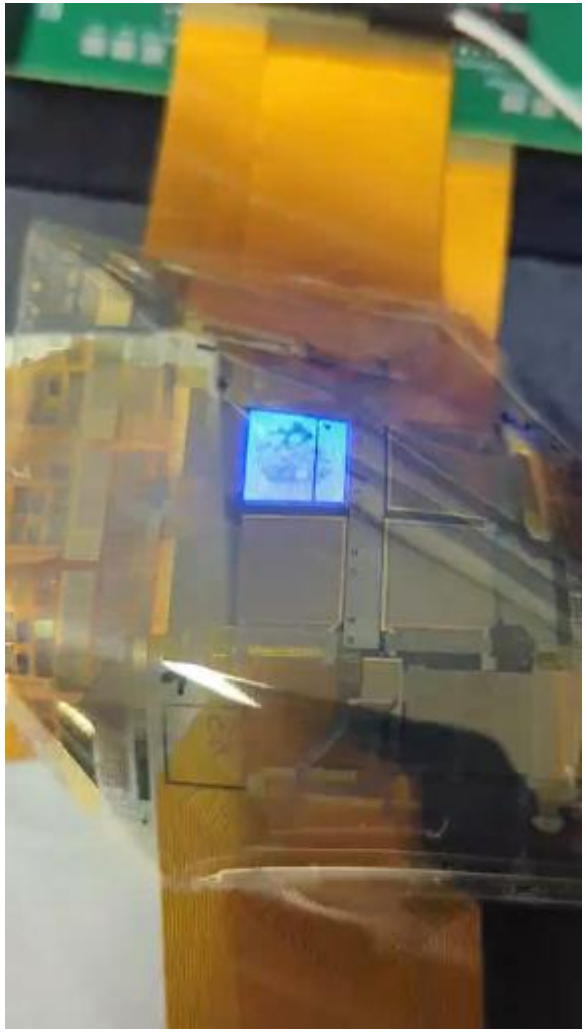


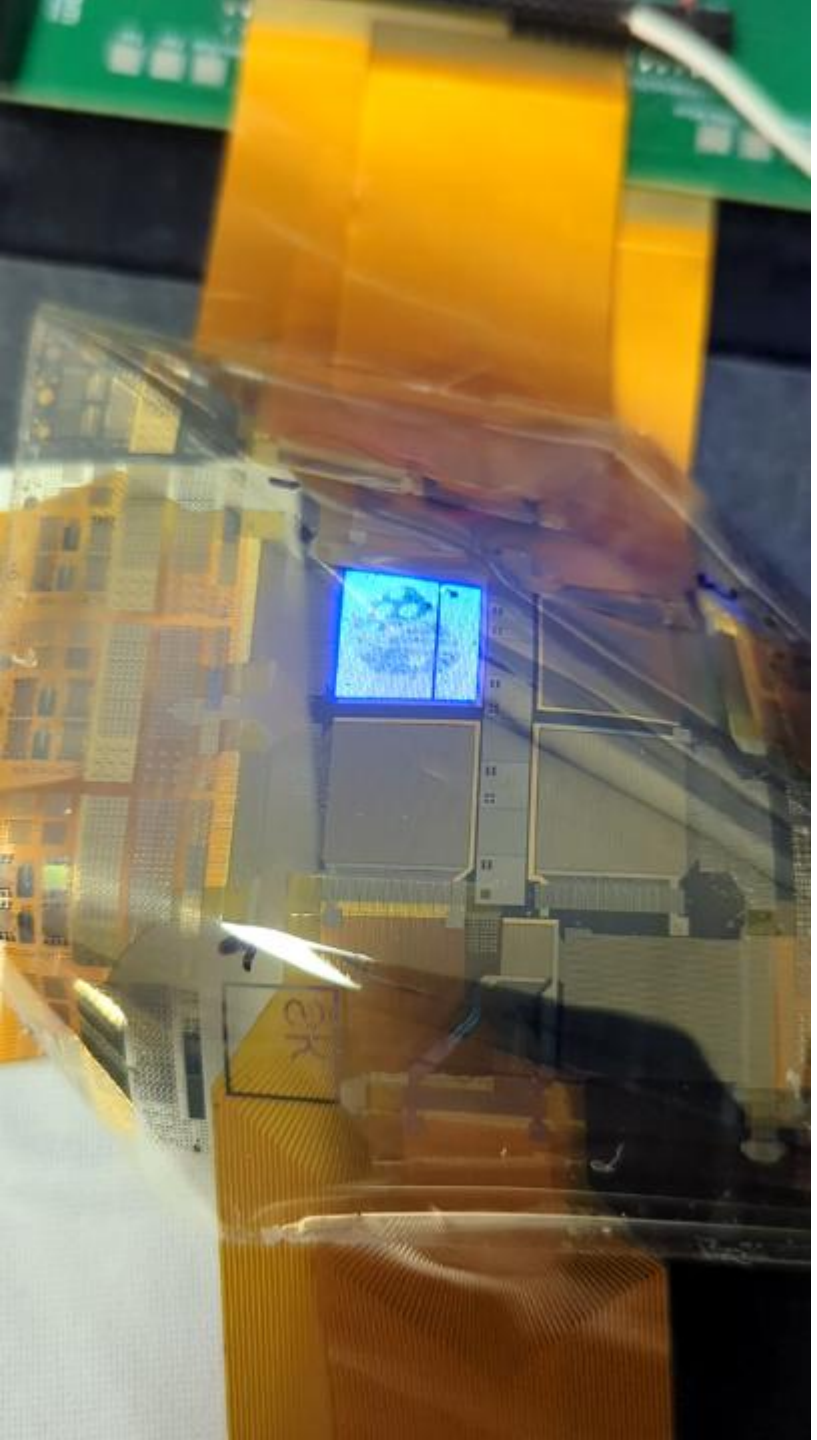
First prototype display fabricated on PEN substrate (laminated on glass)

48x48 resolution

De-mounting of PEN from glass carrier did not appear to affect display performance

Further iterations and improvements in design and fabrication are in progress





Demo

World-first transparent, monolithic OTFT-on-flexible substrate demonstrated on 1st attempt.

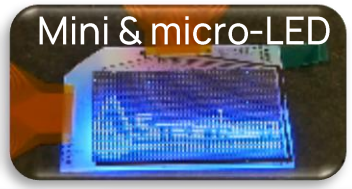
Levels of defectivity are high due to incoming micro-LED yield, Class 1000 “R&D” cleanroom processes, manual transfer process and some design-related factors.

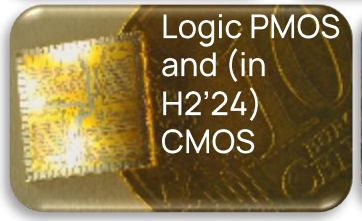
Improvements to incoming sample yield and transfer method, in addition to design improvements should boost performance of next attempt significantly.

Lab to Fab Transition for OTFT products

Stage 1 - 4” or 8” scale Feasibility and innovation

- Digital lithography employed (fast iteration, low cost)
- Key learnings made (design, performance, application “fit” for technology)
- Design for manufacture (process, materials, equipment)
- Proof of concept stage (small functional display or circuit)



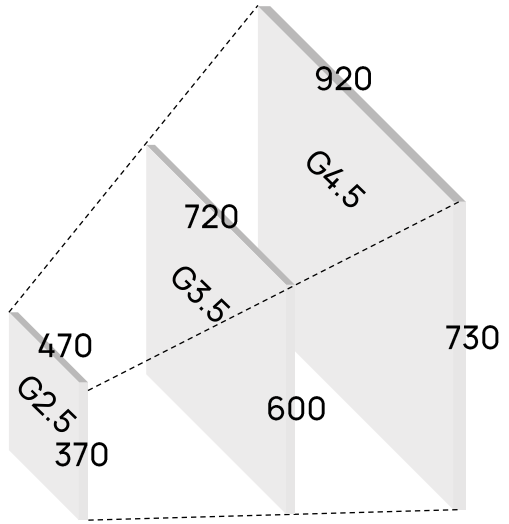


Stage 2 - Gen 2.5 scale Pilot development

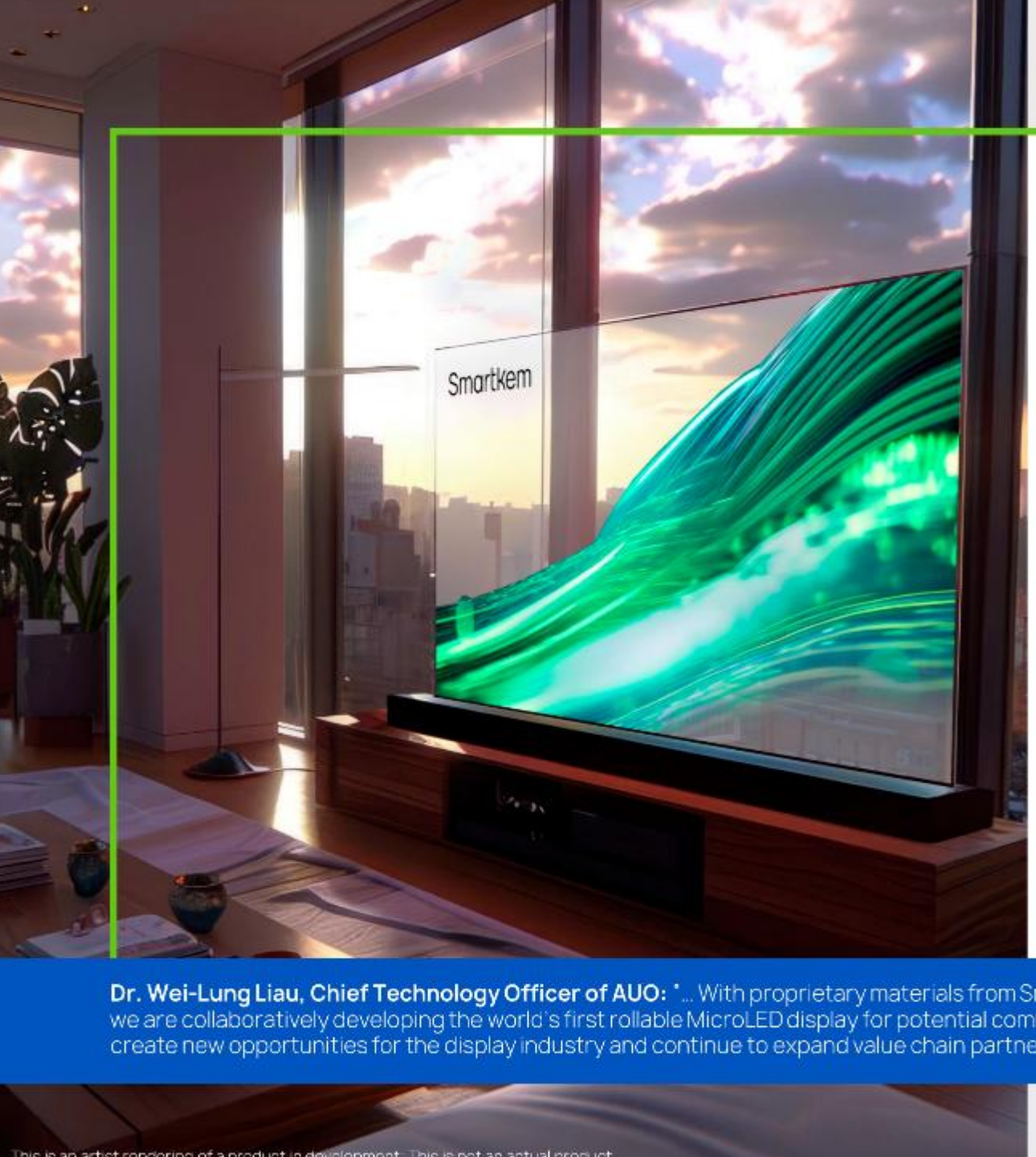
- Process adaptation to industry standard toolset
- Defectivity reduced for displays
- Pilot products used for end user trials
- Product reliability tests
- PDK’s developed for devices

Stage 3 Manufacturing scale-up

- Gen 2.5 or larger
- Technology transfer to display companies
- Manufacturing scale up for new display formats
- Process stabilisation
- New product introduction to market



R&D → Pilot → Manufacturing



AUO Smartkem

Partner to Develop a New Generation Rollable, Transparent MicroLED Display

- AUO is Taiwan's largest display manufacturer
- 1st Smartkem microLED display in development
- To use ITRI's Gen 2.5 assembly line
- Partnership awarded grant by 2024 Taiwan-UK Research & Development Collaboration

Dr. Wei-Lung Liau, Chief Technology Officer of AUO: "... With proprietary materials from Smartkem and the OTFT production process from ITRI, we are collaboratively developing the world's first rollable MicroLED display for potential commercialization with cost advantage. We believe this will create new opportunities for the display industry and continue to expand value chain partner cooperation and influence." *(11/25/2024 press release)*

This is an artist rendering of a product in development. This is not an actual product.

Summary

- Chip first process offers the potential of very high backplane to chip connection yield without time consuming and costly repair processes
- OTFT low temperature processing enables the chip-first approach to be used without micro-LED damage
- Partnership with companies developing micro-LED transfer techniques is essential to move forward the manufacturing of high yield flexible micro-LED displays

Thank you

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