June 16, 2022

QuickLogic and eTopus Announce Disaggregated, Flexible eFPGA Chiplet Template

- Targeting advanced, high-performance applications
- Available initially as configurable IP and later as Known Good Die chiplets

SAN JOSE, Calif., June 16, 2022 /PRNewswire/ -- QuickLogic Corporation (NASDAQ: QUIK), a developer of ultra-low power multi-core voice-enabled SoCs, embedded FPGA IP, and Endpoint AI solutions, and eTopus, a leader in high speed, low latency, low power connectivity IP, today announced the industry's first disaggregated eFPGA-enabled chiplet template solution. Based on QuickLogic's Australis™ eFPGA IP Generator and industry-leading chiplet interfaces from eTopus, the template delivers unprecedented design flexibility and bandwidth for high performance applications.

Unlike discrete FPGAs with pre-determined resources of FPGA LUTs, RAM, and I/Os, the disaggregated eFPGA-enabled chiplet template will be available initially as a configurable IP, and eventually as Known Good Die (KGD) chiplets. Each template will be designed with native support for emerging industry chiplet interfaces including the Bunch of Wires (BOW) and UCIe standards, enabling seamless integration with a customer's own devices. This approach enables customers to size the solution for their needs while being compatible with emerging chiplet standards.

The initial template will use the 6nm process technology to balance performance and cost. eFPGA LUT counts will start at 200K with additional functionality available in block RAM and Digital Signal Processing (DSP) blocks. Surrounding the eFPGA core will be up to 384 Die2Die links developed by eTopus. Each link can run at 0.5/4/8/16G and is organized as a x64 block to efficiently transport ethernet, PCIe, AI/ML, and compute traffic.

"By leveraging our proven Australis eFPGA IP compiler, we are now able to produce

standard eFPGA-enabled chiplet templates as well as more application or customer-optimized chiplet templates in a matter of months," said Brian Faith, president, and CEO of QuickLogic. "This positions our solution to serve a broad range of high-performance, low power applications – enabling our customers to not only size the eFPGA according to their needs, but to focus on what differentiates their products in the market."

eTopus is developing an extended version of the BOW interface as well the new UCIe standard for low power, low latency die-to-die connectivity. It also plans to develop complementary I/O chiplets which will be available as IP and Known Good Die (KGD) with partners.

"We are very excited to support QuickLogic's dis-aggregated eFPGA chiplet template solution," said Harry Chan, CEO of eTopus. "For 6nm, eTopus has existing 112G SerDes for Ethernet IP and PCIe Gen 5 and 6 PHY as well as controllers that are available for design-in now. Our high-speed mixed signal technology will provide the glue to connect QuickLogic's eFPGA chiplets templates to other I/O chiplets and SOCs via our die-to-die technology, which features industry leading latency of <2nS and power <0.25pj/bit."

Availability

Availability of the chiplet template is expected in the first half of 2023. Interested customers can contact QuickLogic at sales@quicklogic.com or eTopus at sales@etopus.com.

About eTopus Technology Inc.

eTopus is the technology leader in high performance, DSP-based, mixed-signal, ultra-high-speed semiconductor interconnect solutions. Our ultra-high-speed SerDes IP is adopted by global Tier-1 players to be used in networking, storage, 5G, and AI applications. eTopus is a VC-backed startup headquartered in Silicon Valley where our innovations and advanced architectures are developed. Our investors include SK Telecom, HK-X, corporate VCs, and cross-border funds. For more information, please visit www.etopus.com.

About QuickLogic

QuickLogic Corporation (NASDAQ: QUIK) is a fabless semiconductor company that develops low power, multi-core semiconductor platforms and Intellectual Property (IP) for Artificial Intelligence (AI), voice and sensor processing. The solutions include embedded FPGA IP (eFPGA) for hardware acceleration and pre-processing, and heterogeneous multi-core SoCs that integrate eFPGA with other processors and peripherals. The Analytics Toolkit from our recently acquired wholly owned subsidiary, SensiML Corporation, completes the end-to-end solution with accurate sensor algorithms using AI technology. The full range of platforms, software tools and eFPGA IP enables the practical and efficient adoption of AI, voice, and sensor processing across mobile, wearable, hearable, consumer, industrial, edge and endpoint IoT. For more information,
visit www.quicklogic.com and https://www.quicklogic.com/blog/.

View original content to download multimedia:https://www.prnewswire.com/news-releases/quicklogic-and-etopus-announce-disaggregated-flexible-efpga-chiplet-template-301569363.html

SOURCE QuickLogic Corporation