Q3 Fiscal 2024 Earnings Conference Call Prepared Remarks

Operator
Ladies and gentlemen, good afternoon.
At this time, I would like to welcome everyone to QuickLogic Corporation's Third Quarter Fiscal 2024 Earnings Results Conference Call. As a reminder, today's call is being recorded for replay purposes through November 18, 2024. I would now like to turn the conference over to Ms. Alison Ziegler of Darrow Associates. Ms. Ziegler, please go ahead.

Alison Ziegler

Thank you, operator, and thanks to all of you for joining us. Our speakers today are Brian Faith, President and Chief Executive Officer, and Elias Nader, Senior Vice President, and Chief Financial Officer.

As a reminder, some of the comments QuickLogic makes today are forward-looking statements that involve risks and uncertainties, including but not limited to stated expectations relating to revenue from new and mature products, including the expected timing of such revenue; statements regarding our future profitability and cash flows; statements regarding the timing, milestones and payments related to QuickLogic’s government contracts; statements pertaining to QuickLogic's future performance, design activity and its ability to convert new design opportunities into production shipments; timing and market acceptance of its customers' products; schedule changes and production start dates that could impact the timing of shipments; the company’s future evaluation systems; broadening the number of our ecosystem partners; and expected results and financial expectations for revenue, gross margin, operating expenses, profitability and cash.

Actual results or trends may differ materially from those discussed today. For more detailed discussions of the risks, uncertainties and assumptions that could result in those differences, please refer to the risk factors discussed in QuickLogic's most recently filed periodic reports with the SEC. QuickLogic assumes no obligation to update any forward-looking statements or information, which speak as of the respective dates of any new information or future events.

In today’s call, we will be reporting non-GAAP financial measures. You may refer to the earnings release we issued today for a detailed reconciliation of our GAAP to non-GAAP results and other financial statements. We have also

posted an updated financial table on our IR web page that provides current and historical non-GAAP data.

Please note, QuickLogic uses its website, the company blog, corporate Twitter account, Facebook page, and LinkedIn page as channels of distribution of information about its business. Such information may be deemed material information, and QuickLogic may use these channels to comply with its disclosure obligations under Regulation FD.

A copy of the prepared remarks made on today's call will be posted on QuickLogic's IR web page shortly after the conclusion of today's earnings call.

I would now like to turn the call over to Brian.

Brian – Chief Executive Officer

Thank you, Alison. Good afternoon, everyone and thank you all for joining our third quarter 2024 conference call.

We have made tremendous progress during the first ten months of 2024, and we have a number of significant contracts in process that we believe we will win in the coming months. The most significant of these contracts that we expected to be awarded earlier this quarter, has been delayed to later this quarter. The primary reason for this delay is its expanded scope.

While this expansion is clearly good news, the delay will push the majority of the revenue recognition into Q1 2025. As a result, our revenue guidance for Q4 will be $6 million. Following my review of major contracts and other updates, Elias will cover our Q4 revenue guidance and other financial measures, which will include our forecasted return to non-GAAP profitability in Q4 and for the full fiscal year 2024.

Last Friday, EE Times published an article announcing that Analog Devices will acquire the assets and technical team from our primary eFPGA IP competitor, Flex Logix.

According to the article, Flex Logix eFPGA IP has been used by ADI for a long time and there is an intent to extend the use of eFPGA across ADI product lines. Based on the information in this article and other inputs, we believe ADI will discontinue external licensing of Flex Logix IP.

With eFPGA customers likely having advance notice of this news, we have seen an influx of inquiries from large companies for applications targeting fabrication processes for which we've already developed eFPGA Hard IP. Given these circumstances, we believe contract negotiations will be fast-tracked and with eFPGA Hard IP already established, we can deliver customer-specific IP quickly.

Also very notable is the fact Flex Logix was the only other eFPGA company that was announced as a member of both the Intel Foundry's Accelerator IP and US Military / Aerospace / and Government or USMAG Alliances. This bolsters our confidence that our early investments to develop eFPGA Hard IP for Intel 18A will pay off in a big way.

On June 18th we announced that we joined the Intel Foundry's Accelerator IP and USMAG Alliances.

Driven by customer demand and to capitalize on the already considerable interest from companies targeting Intel 18A for new designs, we initiated development of our eFPGA Hard IP in Q2. We believe this will position QuickLogic to be the first available source for eFPGA Hard IP optimized for Intel 18A.

We already have two outstanding proposals for Intel 18A designs in the Defense Industrial Base sector; one of which is very significant. We are also in discussions with a very large company in the Compute / IT sector that we believe will lead to a formal proposal in the near-term.

Due to our early investments to develop eFPGA Hard IP and our unique ability to quickly convert that to customer-specific Hard IP cores, we believe we are well positioned to win Intel 18A contracts and accelerate the schedule of our deliverables.

On July 8th we announced the award of the third tranche of the Strategic Radiation Hardened FPGA government contract.

We anticipate the fourth tranche will be awarded this quarter and expand the scope of the long-term contract that was initiated in 2022. The total potential for this contract, including future options, is $72 million. If these options are exercised, we expect the funding rate will increase beginning in 2025.

During the first quarter of 2024 we announced two contracts that will be fabricated using a 12nm process.

The first contract, is with a Defense Industrial Base customer and includes two cores that will be fabricated on GlobalFoundries™' 12LP process. As we forecasted last quarter, we completed our initial deliverables for the first core during Q3 and are on schedule to complete our work on the second core during Q4. We anticipate further revenue recognition in Q2 2025 as the customer does test-chip preparation.

The second contract, is with a large, well-known, international company. This design is for a new ultra-low-power SoC that is targeting a variety of commercial and industrial IoT AI applications. This design will be fabricated by TSMC on its 12nm process.

We completed our deliverables on this contract and recognized the associated revenue during Q3. We believe we'll have more clarity about the potential of a second design once the test-chip for the first design is completed during Q1 2025.

In November 2022, I shared that we taped out a new device for a customer that incorporates our eFPGA Hard IP. This contract was announced in June 2022 with the stated expectation that revenue would extend to June 2025 with follow-on Storefront revenue expected after the completion of the IP contract.

In line with what I covered during our last conference call, due to a delay with one of the customer's subcontractors, we believe we will resume work on this design during the second half of 2025.

This program is still a solid go and could represent tens of millions of dollars in Storefront revenue starting in a couple of years.

In September 2023 we announced a leading technology company chose our eFPGA Hard IP for a design that will be fabricated using GlobalFoundries 22FDX™ platform.

The customer has completed its design, expects to tape-out later this quarter and receive test-chips from GlobalFoundries during the first half of 2025. If all goes as planned, that will lead to our revenue recognition of a production license during the second half of 2025.

In November 2023 we announced a global semiconductor leader chose our eFPGA Hard IP for a design that will be fabricated on UMC's 22nm process. We delivered our IP earlier this year and test-chip evaluations are going very well.

We anticipate being involved in their marketing efforts during Q4 2024 and Q1 2025. We expect these efforts will generate IP revenues for QuickLogic in 2025 and royalty revenue beyond.

In addition to these awarded contracts, we have a number of large contract proposals pending, some valued in the mid-seven-figures. These include proposals on a variety of Critical Infrastructure sectors and a proposal with a large semiconductor company. Some of these proposals are potential Storefront designs.

In total, we have delivered our Australis generated eFPGA Hard IP on five unique process technologies funded by customer contracts. These include GlobalFoundries 12LP, TSMC 12nm, GlobalFoundries 22FDX, UMC 22nm and SkyWater RH90. Additionally, we believe we are on track to be the first company to offer eFPGA Hard IP for Intel 18A.

Given the fact these include some very popular high-volume process technologies, this is a big deal. Once we establish our eFPGA Hard IP for a given process technology, our proprietary Australis eFPGA Hard IP generator can deliver customer specific eFPGA Hard IP rapidly, in some instances, within days.

This positioning provides multiple advantages. First, it enables us to further leverage the investments we've made to establish eFPGA Hard IP for a given process technology. Second, it enables us to respond quickly to opportunities, and that lowers our costs associated with proposals.

Third, it increases our market reach as potential customers know we have a proven solution that can be deployed in a very short period of time. We expect these benefits will accelerate our growth, profitability, and market penetration.

To that point, I'm often asked about the market sectors we are serving. As it stands today, we have active production IP contracts in the DIB, Communications and Industrial sectors, and a test-chip IP contract in the Mass-Transportation sector. In addition to these, we have outstanding production IP proposals in the DIB, Communications, Industrial, Compute, IT and Mass-Transportation sectors.

These market sectors, which fall under the Critical Infrastructure umbrella, share common traits. They all have long design cycles, very long production lifecycles, are pervasive users of programmable logic and ASICs, and are more focused on capabilities than cost. You will see examples of Critical

Infrastructure applications we are targeting on our updated website that will go live later this month.

The U.S. Department of Defense and Department of Commerce fund a variety of contracts to advance technology. The primary focus for the DoD is to fund product developments that will be used by its DIB contractors. The Department of Commerce has a broader agenda.

We have three outstanding proposals for advanced technology initiatives that fit well in with our core business strategy.

In addition to our proposal for the fourth tranche of the Strategic Rad Hard contract that we won as the Prime Contractor in 2022, we also have two proposals pending where we partnered with very large companies that submitted the bids as the Prime Contractor. These proposals, while exciting, are too early in the process to expand upon.

In past conference calls I referenced two Chiplet proposals as having a combined potential value of $40 million. We recently learned that we were not selected. As best we can tell, these proposals did not elect to incorporate FPGA technology. The value of these proposals has been removed from our funnel and only partially replaced with new opportunities. As a result, our funnel value as of today is $164 million.

The shiny side of this coin is that several of the new opportunities are inbound inquiries from very large companies for fully funded programs that have committed to using eFPGA and are targeting fabrication processes for which we already have eFPGA Hard IP. Due to these factors, I believe our odds of winning are very high, and in at least one case, the contract could move forward quickly.

We remain very optimistic about the future of Merchant Chiplet designs. Chiplets are already being used by large semiconductor companies like AMD, Intel, and NVIDIA in high volume, but for the most part, these are vertically integrated designs.

In my recent communication with Kash Johal, CEO of YorChip, he stated that Merchant Chiplet designs will build traction in 2026, and he believes that together we are well positioned to be a leader in low-power edge designs that require programmability.

We anticipate the first jointly developed eFPGA Chiplet integrating QuickLogic IP in the second half of 2025. Going forward, this eFPGA Chiplet product line will be expanded to include devices ranging from 40K LUTs to over one million

LUTs. All of these designs will use the industry standard high-speed UCIe Chiplet interface, which is supported by most of the largest tech companies in the world.

In line with our earlier forecasts, shipments of EOS S3 to our lead smartphone customer increased during the first half of 2024 and as we forecasted, Q3 should be the low point for the year. We anticipate shipments will sequentially increase in Q4 and again in Q1 2025. In a recent meeting at our headquarters, our customer identified new designs that could extend revenue into 2026.

Consistent with our prior outlook, we are forecasting a modest increase in display bridge and mature product shipments for full-year 2024.

In our last conference call, I discussed three new distribution agreements intended to expand our coverage internationally and enhance our coverage of the U.S. DIB. In October, we added Magenta to broaden our coverage in Turkey and UAE. Magenta specializes in customer specific solutions for military and aerospace companies.

The unique market focus and capabilities of these distributors is already yielding results. In the short time since they have joined the QuickLogic team, they have collectively initiated several well-qualified eFPGA IP design opportunities with a combined value of approximately $2.5 million. They are also working with customers on new discrete FPGA and EOS S3 opportunities.

Aurora is our comprehensive software Tool Suite comprised of Open Source and proprietary components that is used by our customers for eFPGA design. It provides seamless integration from customer RTL to eFPGA / FPGA Bitstream.

In line with our previous forecast, we released V2.8 during Q3 and are scheduled to release V2.9 during Q4. Driven by current strategic customer demand, we have entered into a contract with Synopsys to license its Synplify FPGA synthesis software. We will integrate Synplify in our Aurora Tool Suite for lead customer beta testing this quarter with full release expected in Q1 2025.

Synopsys will enhance its Synplify tools to support our unique QuickLogic eFPGA architecture, which will enable customers that use Synplify to work in a familiar design flow environment. Synplify will also enable customers to further optimize QuickLogic eFPGA designs for Power, Performance and Area; broadly known as PPA. In some applications, these are critical factors, so integrating Synplify will expand our available markets.

Turning now to SensiML

As we covered in our last conference call, SensiML has launched Piccolo AI™, the first complete, open-source AutoML solution for the development of edge AI/ML applications. SensiML also launched its Generative AI feature that enables developers to rapidly build ML training datasets for custom voice recognition, voice command and speaker identification applications.

Through a close collaboration with SensiML, Efabless announced last month the launch of chipIgnite ML, a new system-on-chip (SoC) platform that is optimized for SensiML software. The prototype run of this new SoC solution is scheduled for April 2025 with production to follow.

On October 10th, SensiML announced its support for RISC-V. With RISC-V support, developers can now use SensiML's open-source Piccolo AI™ AutoML tool to create ultra-efficient machine learning models tailored to specific applications using open-source RISC-V hardware.

SensiML is collaborating with two top-tier microcontroller companies to enable its AI / ML development tools on their edge platforms and planned AI accelerator SoCs.

With that, let me now turn the call over to Elias for a review of the financial results, and I will rejoin for our closing remarks. Elias, please go ahead.

Elias– Chief Financial Officer

Thank you, Brian and good afternoon, everyone.

Total third quarter revenue was $4.3 million and slightly above the midpoint of our revenue guidance. Total revenue was down 36% from Q3 2023 and up 4% compared to Q2 2024.

New product revenue in Q3 was $3.5 million, down 42% from Q3 last year and up 16% compared to Q2. Mature product revenue was $0.7 million, up from $0.6 million in Q3 last year and down from $1.1 million in Q2 2024.

The decreases in total revenue and new product revenue from the same period a year ago were mostly due to the timing of certain large eFPGA IP contracts.

Non-GAAP gross margin in Q3 was 60% and at the top end of our outlook range. This compared with non-GAAP gross margin of 78% in Q3 last year and 53.1% in Q2.

Non-GAAP operating expenses in Q3 were approximately $3.3 million and at the top end of our outlook range. This compares with non-GAAP operating expenses of $3.3 million in the third quarter last year and $2.9 million in the second quarter of 2024.

The noted deviations from the midpoints of our outlook are mainly attributable to the allocation of R&D between operating expenses and COGS. Accurately projecting the distribution of R&D costs between these categories remains an ongoing challenge. However, at the operating line on our income statement, these allocations ultimately balance out.

Non-GAAP net loss was $0.9 million, or $0.06 cents per share. This compares to non-GAAP net income of $1.8 million, or $0.13 cents per share, in last year's third quarter, and a non-GAAP net loss of $0.7 million, or $0.05 cents per share, in the second quarter of fiscal 2024.

For the third quarter, two customers accounted for 10% or more of our revenue.

At the close of Q3, total cash was $22.4 million compared with $23.3 million at the close of Q2. These figures include our $20 million credit facility.
Cash usage during Q3 was slightly higher than our outlook and is mostly attributable to the timing of our Strategic Radiation Hardened contract and payments to our subcontractors.

Please keep in mind, cash use during Q3 was impacted by the advanced investments we're making to establish eFPGA Hard IP for Intel 18A and Synopsys Synplify software ahead of contracts. We are anticipating significant IP contract awards that will leverage these investments later this quarter and in Q1 2025.

Now moving to our guidance and outlook for the fourth quarter of fiscal 2024, which will end on December 31, 2024:

Revenue guidance for Q4 2024 is approximately $6 million, plus or minus 10%. Fourth quarter revenue is expected to be comprised of approximately $5 million in new products and $1 million in mature products.

As Brian stated in his remarks, our lower than anticipated Q4 revenue guidance is attributable to the delay of certain IP contracts that we thought

would be awarded earlier this quarter. The most significant of these contracts was delayed due to the scope of the contract being expanded. We anticipate it will be awarded later in Q4, which will push the majority of the revenue recognition into Q1 2025.

Based on the anticipated Q4 revenue mix, non-GAAP gross margin for the fourth quarter is expected to be approximately 60%, plus or minus 5 percentage points.

Our non-GAAP operating expenses are expected to be approximately $3.3 million, plus or minus 10%.

Please note that given the nature of our industry, we may occasionally need to reclassify certain expenses to COGS or capitalize certain costs. The reclassifications are mainly related to labor and tooling for our revenue contracts with customers. Such capitalization may reduce OPEX and alter the timing for recognizing the corresponding expenses in COGS. This may cause variability in our gross margins and operating results.

Bearing these factors in mind and based on our current full-year revenue outlook, we believe our full-year 2024 non-GAAP gross profit margin will be approximately 60%.

After interest and other income, we currently forecast that our Q4 non-GAAP net income will be approximately $0.35 million to $0.48 million, or approximately $0.02 cents to $0.03 cents per share, based on roughly 14.8 million fully diluted shares.

Based on our outlook for Q4, after interest, other income, and taxes, we expect full-year FY24 non-GAAP net income will be approximately $0.33 million to $0.45 million or $0.02 cents per share to $0.03 cents per share based on an estimated 14.5 million diluted shares.

The difference between our GAAP and non-GAAP results is related to non-cash, stock-based compensation expenses. In Q4, we expect this compensation will be approximately $1.1M, similar to Q3.

As a reminder, there will be movement in our stock-based compensation during the year and it may vary each quarter based on the timing of grants to employees.

At the midpoint of our outlook for Q4, we expect cash usage to be under $500 thousand. Based on our outlook for new contracts and the timing of forecasted

deliverables, we believe Q4 will mark the low point for net cash and that Q1 2025 will be cash-flow positive.

Please note, we will continue to invest in developing eFPGA Hard IP for Intel 18A as well as with Synopsis for Synplify software in Q4. We believe this provides us with strategic advantages in winning contracts, some of which are pending, and will shorten the time it takes us to recognize revenue once contracts are awarded.

With that, let me now turn the call back over to Brian for his closing remarks and thank you very much.

Brian – Chief Executive Officer

Summation

Thank you, Elias. And thank you and your team for tight management of our finances that we believe will result in our second consecutive year of profitability.

While the delays we've encountered in finalizing new contracts have reduced our revenue outlook for 2024, I believe that trend will change beginning this quarter and continue into 2025.

In addition to the contracts, we've had in the works for a number of months, we have also seen an influx of well qualified inquiries during the last several weeks that are attributable to end customers learning about the acquisition of Flex Logix prior to the formal announcement.

In some cases, we believe the customers would like to move forward quickly and we have the resources in place to support that.

As I noted earlier, we have eFPGA Hard IP ready for five fabrication processes that were all funded by customer contracts. We are also on schedule to have our internally funded eFPGA Hard IP for Intel 18A completed in Q1.

With our Hard IP already ported to these process nodes, we can develop customer-specific variants in a matter of weeks using our proprietary Australis eFPGA IP Generator. We are the only company in the world capable of executing this quickly and efficiently, and our track record of on-time delivery proves it.

We are also the only eFPGA IP company in the world that has the resources, knowledge, and business relationships to provide our customers with a turnkey Storefront solution.

Managing the manufacturing and test flow for semiconductor devices is complex and seldom the core competency for our ASIC customers. With over three decades of experience in the merchant semiconductor device market, we offer these customers a unique, low-risk and trusted solution.

This is a huge deal that has the potential to exponentially expand the scope and size of QuickLogic.

Before I turn the call over for Q&A, I would like to pause for a moment to pay respect to and express our gratitude for our Veterans dedicated and selfless service to our Country. This includes several members of my own family, both past and present.

Closing Remarks

Thanks again for joining us today. Hopefully we will connect with some of you at one of our upcoming events including the Craig Hallum Alpha Select 1x1 Conference in New York on November 19th or the semiconductor-focused Annual NYC Summit, also in New York, on December 17th.

Have a good day!