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Intel Foundry Details Process Milestones and Future Innovation at VLSI Symposium

SANTA CLARA, Calif.--(BUSINESS WIRE)-- At the 2026 VLSI Symposium, Intel Foundry provided an update on its process roadmap and long-term innovation investments. It shared that Intel 18A-P, the first performance enhancement in the Intel 18A family, has entered risk production, meeting the timeline first shared with customers and partners last year.

“Our updates and presentations at VLSI signal to Intel Foundry customers and partners that we are fully committed to leading edge process innovation over the long term,” said Naga Chandrasekaran, executive vice president and general manager of Intel Foundry. “This is a journey, and while we have more work ahead, we appreciate the opportunity to share the progress we are making with Intel 18A-P and our longer-range R&D.”

Intel 18A-P updates at VLSI

Intel Foundry enables Intel 18A-P performance, power and design benefits through a mix of transistor, interconnect, and design-technology co-optimizations. At VLSI, engineers from Intel Foundry detailed the following advancements:

- Intel 18A-P delivers 9% higher performance at iso-power or 18% lower power at iso-performance compared to Intel 18A, alongside enhanced thermal characteristics and expanded design flexibility.
- Unveiled Power Boost, Intel 18A-P’s new dual contact, low resistance transistor option enabling increased drive current and greater frequency at matched capacitance.
- 20-40% improved thermal resistance through both materials and design innovations.
- 10-30% improved via resistance (referring to the vertical connections between the layers of a chip) using geometric and materials optimizations.
- Mobility enhancement through PMOS via strain engineering, letting current move through the transistor more efficiently.
- New low power and high-performance transistor options.
- New fifth logic Vt pair between ULVT and LVT (an additional fifth Vt option for designers to balance speed and power).
- Intel 18A-P is fully design rule compatible with Intel 18A, enabling straightforward reuse of existing IP and design flows.
- Similar to Intel 18A, Intel 18A-P offers two cell heights (180nm and 160nm), a contacted poly pitch of 50nm.

Additional updates at VLSI

Intel Foundry brought gate-all-around (GAA) transistors and backside power delivery (BSPD) to market last year with Intel 18A. This week, engineering teams discussed how these technologies provide the foundation for improved performance, energy efficiency and scaling for future logic designs:

- In a VLSI invited talk, Intel Foundry Vice President and Fellow Eric Karl showed how the company is quantifying the advantages of backside power delivery and gate-all-around transistors. Karl discussed 11% routed area reduction and 10X dynamic voltage droop reduction, enabling up to 6% frequency uplift or greater than 15% dynamic power reduction versus a comparable frontside interconnect technology.
- Manju Shamanna from Intel Foundry's Silicon and Platform Engineering group shared silicon results from CPU cores built on a gate-all-around and backside power delivery process. His research demonstrates stronger frequency scaling at lower voltages, including ~ 30% frequency improvement at low voltage (~0.5V), while also reducing IR drop and enabling more efficient operation.

Future innovation at VLSI

Intel Foundry also presented long-term research updates at the event, across several areas important to future silicon scaling:

- CFET (Complementary FET): Intel demonstrated monolithic CFET inverters with vertically stacked NMOS and PMOS devices at a 45nm gate pitch, advancing a path to continue logic scaling beyond gate all around transistors through vertical device architecture.
- GaN + Si integration for power management: Intel demonstrated 300mm monolithic integration of gallium nitride power devices with silicon logic, including a ~1,000 gate digital control block, enabling efficient, large scale digital control alongside high performance power devices in a single process and reducing system complexity.
- Subtractive ruthenium interconnect: Intel demonstrated subtractive ruthenium with airgap integration, achieving up to ~35% capacitance reduction and measurable frequency gains versus copper, pointing to a viable path for improved resistance capacitance scaling as interconnects continue to shrink.

Learn more about Intel Foundry's VLSI updates and presentationshere.

Forward-Looking Statements

This release contains forward-looking statements that involve a number of risks and uncertainties. Words such as "accelerate", "achieve", "aim", "ambitions", "anticipate", "believe", "committed", "continue", "could", "designed", "estimate", "expect", "forecast", "future", "goals", "grow", "guidance", "intend", "likely", "may", "might", "milestones", "next generation", "objective", "on track", "opportunity", "outlook", "pending", "plan", "position", "possible", "potential", "predict", "progress", "ramp", "roadmap", "seek", "should", "strive", "targets", "to be", "upcoming", "will", "would", and variations of such words and similar expressions are intended to identify such forward-looking statements, which may include statements regarding:

- Our Intel 18A-P process node and risk production of such node, including the performance, power and design benefits, competitiveness and technological advancements;
- Our research developments in CFET inverters, GaN + Si Integration and sRu interconnects.

Such statements involve many risks and uncertainties that could cause our actual results to

differ materially from those expressed or implied, including those associated with:

- the high level of competition and rapid technological change in our industry;
- the significant, long-term and inherently risky investments we are making in R&D and manufacturing facilities that may not realize a favorable return;
- the complexities and uncertainties in developing and implementing new semiconductor products and manufacturing process technologies;
- changes in product demand and margins;
- macroeconomic conditions and geopolitical tensions and conflicts, including geopolitical and trade tensions between the U.S. and China, tensions and conflict affecting Israel and the Middle East, rising tensions between mainland China and Taiwan and the impacts of Russia's war on Ukraine;
- recently elevated geopolitical tensions, volatility and uncertainty with respect to international trade policies, including tariffs and export controls, impacting our business, the markets in which we compete and the world economy;
- the evolving market for products with AI capabilities;
- our complex global supply chain supporting our manufacturing facilities and incorporating external foundries, including from disruptions, delays, trade tensions and conflicts, or shortages;
- product defects, errata and other product issues, particularly as we develop next-generation products and implement next-generation manufacturing process technologies; and
- other risks and uncertainties described in this report, our 2025 Form 10-K and our other filings with the SEC.

Given these risks and uncertainties, readers are cautioned not to place undue reliance on such forward-looking statements. Readers are urged to carefully review and consider the various disclosures made in this release and in other documents we file from time to time with the SEC that disclose risks and uncertainties that may affect our business.

Unless specifically indicated otherwise, the forward-looking statements in this release do not reflect the potential impact of any divestitures, mergers, acquisitions or other business combinations that have not been completed as of the date of this filing. In addition, the forward-looking statements in this release are based on management's expectations as of the date of this release, unless an earlier date is specified, including expectations based on third-party information and projections that management believes to be reputable. We do not undertake, and expressly disclaim any duty, to update such statements, whether as a result of new information, new developments, or otherwise, except to the extent that disclosure may be required by law.

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