Third Quarter 2025 Earnings Conference Call Prepared Remarks

Operator

Ladies and gentlemen, good afternoon.
At this time, I would like to welcome everyone to QuickLogic Corporation's Third Quarter Fiscal 2025 Earnings Results Conference Call. As a reminder, today's call is being recorded for replay purposes through November 18, 2025. I would now like to turn the conference over to Ms. Alison Ziegler of Darrow Associates. Ms. Ziegler, please go ahead.

Alison Ziegler
Thank you, Vaughn, and thanks to all of you for joining us. Our speakers today are Brian Faith, President and Chief Executive Officer, and Elias Nader, Senior Vice President, and Chief Financial Officer.

As a reminder, some of the comments QuickLogic makes today are forward-looking statements that involve risks and uncertainties, including but not limited to statements regarding our future profitability and cash flows, expectations regarding our future business and statements regarding the timing, milestones, and payments related to our government contracts, statements regarding the use of the Company's ATM program, and statements regarding our ability to successfully exit SensiML.

Actual results may differ due to a variety of factors including: delays in the market acceptance of the Company's new products; the ability to convert design opportunities into customer revenue; our ability to replace revenue from end-of-life products; the level and timing of customer design activity; the market acceptance of our customers' products; the risk that new orders may not result in future revenue; our ability to introduce and produce new products based on advanced wafer technology on a timely basis; our ability to adequately market the low power, competitive pricing and short time-to-market of our new products; intense competition by competitors; our ability to hire and retain qualified personnel; changes in product demand or supply; general economic conditions; political events, international trade disputes, natural disasters and other business interruptions that could disrupt supply or delivery of, or demand for, the Company's products; and changes in tax rates and exposure to additional tax liabilities.

For more detailed discussions of the risks, uncertainties and assumptions that could result in those differences, please refer to the risk factors discussed in QuickLogic's most recently filed periodic reports with the SEC. QuickLogic assumes no obligation to update any forward-looking statements or information, which speak as of the respective dates of any new information or future events.

In today's call, we will be reporting non-GAAP financial measures. You may refer to the earnings release we issued today for a detailed reconciliation of our GAAP to non-GAAP results and other financial statements. We have also posted an updated financial table on our IR web page that provides current and historical non-GAAP data.

Please note, QuickLogic uses its website, the company blog, corporate Twitter account, Facebook page, and LinkedIn page as channels of distribution of information about its business. Such information may be deemed material information, and QuickLogic may use these channels to comply with its disclosure obligations under Regulation FD.

A copy of the prepared remarks made on today's call will be posted on QuickLogic's IR web page shortly after the conclusion of today's earnings call.

I would now like to turn the call over to Brian.

Brian Faith, CEO

Thank you Alison, Good afternoon everyone, and thank you all for joining our third quarter 2025 conference call.

We have made very significant progress since our August conference call. Last quarter I stated that we focused considerable engineering resources to accelerate Storefront design wins for our Strategic Rad Hard FPGA and expand our served available market to include very high-density eFPGA Hard IP designs targeting advanced fabrication nodes. I'm proud to say our engineering team has executed beautifully and we are realizing these goals.

- We expect to begin recognizing Storefront revenue in early 2026 and that it will provide a meaningful contribution to total 2026 revenue

- The interest from large Defense Industrial Base (DIBs) in the SRH Test Chip we funded is notably higher than I anticipated
- We have significantly expanded our ability to address the lucrative markets for very high-density discrete FPGAs and ASICs that require large blocks of eFPGA.
- New contracts and engagements are for much larger blocks of eFPGA and on advanced fabrication processes
- The value contribution of eFPGA in customer designs has grown substantially
- Our penetration in Commercial market sectors is expanding, and with this progress,
- The rate of new contract closure is accelerating to the point that license revenue may surpass NRE revenue for the first time this quarter
- We believe these trends will accelerate going forward

Before I get into the tangible data that support these points, I want to take a moment and provide some color for the revenue guidance Elias will share in his presentation. Based on our backlog and forecasts provided to us by our customers, we are targeting total revenue of $6 million for Q4.

The majority of the contracts that support this outlook are already on the books or have been forecasted by customers to be awarded during the coming weeks. However, a contract valued at nearly $3 million for a commercial application targeting an advanced fabrication node has been forecasted by the customer to be awarded late in the quarter.

If this contract is awarded on or very near the date forecasted, we will be able to recognize a large portion of that revenue in Q4, and with that, realize

our $6 million objective. We have a very high level of confidence in winning this contract, but note that it could push into Q1 2026, and that would result in lower Q4 2025 total revenue. Due to this, Elias will present an unusually wide guidance range.

And now, let's walk through our accomplishments:

In early August, we delivered design files to GlobalFoundries® to fabricate our SRH FPGA Test Chip using its 12LP process. This Test Chip was designed to meet the requirements of certain large DIBs that have programs in development today that are good candidates for this device.

We expect delivery of Test Chips in early Q1 2026 and believe we will have our SRH Dev Kit ready for shipment to customers shortly thereafter.

This initiative was financed by QuickLogic and is independent from our contract with the U.S. Government. Our decision to invest the money and resources to develop this Test Chip was based on our belief that it is critical in our quest to secure strategic design wins and accelerate our Storefront business model.

Since our last earnings conference call, I have personally met with a number of the DIBs that worked with us through the development process, and I cannot emphasize enough the potential of our SRH Storefront initiative. In prior meetings all I had to show were PowerPoint presentations, and now with a Test Chip in fabrication the level of enthusiasm is palpably higher.

As a matter of fact, we already have commitments for SRH Dev Kit orders that we expect to receive by the end of this month. I see this as our first

tangible step towards the hundreds of millions of dollars in potential Storefront business we could win in the coming years.

The importance of demonstrating our SRH FPGA Test Chip goes well beyond the Storefront designs we believe it will enable us to secure. FPGA is the number one spend category for semiconductor devices by the Defense Industrial Base and custom ASICs are a close second. Together, we believe these two categories make up roughly half of the DIB semiconductor TAM.

We expect many of the new strategic designs that require various levels of radiation hardness will use either discrete FPGA devices that we can Storefront or eFPGA Hard IP we can license in new ASIC designs. By delivering a discrete SRH FPGA Test Chip fabricated on the 12LP process we are demonstrating the broader capability of our eFPGA Hard IP for ASIC applications that will meet program requirements ranging from radiation tolerant to strategic rad hard.

There are three very important points I want to highlight here.

- First, DIBs are already using GlobalFoundries' 12LP fabrication process for radiation tolerant and SRH ASICs.

- Second, Government contracts require the use of onshore fabrication for strategic programs when devices are available. As it stands today, we will be the only source for Strategic Rad Hard FPGAs and SRH eFPGA Hard IP that is fabricated in the U.S. by a U.S. company.

- Third, in my meetings at large DIBs, engineering managers have clearly stated that being able to design with our Aurora FPGA User

Tools for both our SRH discrete FPGAs and our eFPGA Hard IP in ASIC designs is a huge plus.

During our last conference call, I stated that Q3 would mark the low point for revenue recognition for our U.S. Government SRH FPGA contract this year. Funded by the current tranche, revenue recognition from the contract will rebound significantly in Q4. Beyond that, we anticipate an increase in quarterly revenue recognition in 2026 that will be funded by the next tranche.

During our last conference call, I forecasted the award of a mid-seven-figure contract from a DIB during Q4 that targets Intel 18A. Unfortunately, there has been a delay in funding that pushes this contract into 2026. We are highly confident that we'll be awarded this contract, but at this juncture, our customer has limited visibility on the timing of funding.

While we await funding for this 7-figure deal, it is worth noting that we have already been awarded multiple contracts by this strategic customer during 2025.

We delivered customer-specific eFPGA Hard IP for this customer's first Intel 18A Test Chip last April. We expect to receive our allocation of Test Chips from this contract during Q1 2026 for our internal verification and characterization. We were subsequently awarded a mid-six-figure contract for a second Intel 18A Test Chip. We delivered customer-specific eFPGA Hard IP for this Test Chip during Q3.

In addition to these Intel 18A Test Chip contracts, during our last conference call, I announced this customer awarded us a contract for a One Million LUT

Feasibility Study that we are scheduled to deliver next week. We are anticipating a follow-on order in the coming weeks associated with this Feasibility Study that will enable the customer to tape out a very high density Intel 18A proof of concept device during the second half of 2026.

The architectural changes we implemented in this Feasibility Study can be leveraged across all advanced fabrication nodes, which we define as 12nm and below. With these changes we can now address the lucrative markets that require very high-density eFPGA blocks in ASIC designs and very high-density discrete FPGAs. This significantly expands our SAM for eFPGA Hard IP and discrete devices, including our SRH FPGA, Chiplets and other Storefront opportunities.

We initiated our Digital Proof of Concept Chiplet program earlier this year as a strategy to accelerate our Storefront Chiplet initiative. Internally, we refer to this as POC. With the support of our large strategic partners, we have leveraged our existing eFPGA Hard IP and readily available 3rd party IP to move forward rapidly and with minimal investment.

In line with the forecast I shared in our last conference call, we completed the initial phase of the Digital FPGA Chiplet POC, where the eFPGA IP is connected to UCIe IP and the necessary interface logic for the IPs to communicate. This digital simulation of the POC is available now and can be further developed to meet different customer requirements. Together with our ecosystem partners, we are engaging with prospective customers in the defense, aerospace, industrial and commercial markets.

We plan to move forward with the next phases of the FPGA Chiplet POC once external funding is committed. This phase will include incorporating

additional IP such as programmable GPIOs, AXI bus, DSPs, data converters and interfaces such as PCI Express, to meet specific customer requirements. We are optimistic that our POC initiative will lead to Storefront revenue in 2026.

On October 2nd we announced a new $1 million eFPGA Hard IP contract for a high-performance Data Center ASIC that will be fabricated on TSMC's 12nm process. In this ASIC, our eFPGA Hard IP will be the primary IP in the design.

This contract is a great illustration of our success in several of the points I mentioned earlier.

- The need for larger blocks of eFPGA
- The increasing value contribution of eFPGA in customer designs
- Winning contracts for designs targeting advanced fabrication processes, and
- Our growing success in commercial market sectors

We will soon announce the expansion of our involvement with a DIB that specializes in cyber-security for strategic and tactical weapons systems. This DIB designs Secure System-on-a-Chip processors that leverage the enhanced security that only eFPGA can provide.

Running these processes in hardware is inherently more secure than software solutions. With eFPGA at the heart of the designs the hardware can be altered to respond to new threats and updated algorithms. We are proud to have been chosen as a trusted supplier of eFPGA Hard IP for these designs.

Last April we announced an eFPGA Hard IP contract with a new Defense Industrial Base customer valued at $1.1 million that will be fabricated on the GF 12LP process. This application utilizes a large block of our eFPGA Hard IP for critical functions, which is a trend we are seeing, particularly in designs targeting advanced fabrication nodes.

With the cooperation of this DIB and its end-customer, we are leveraging the large eFPGA core into a new seven-figure contract we expect to announce in the coming weeks.

In the scope of this new contract, we will be provided with Test Chips that we will incorporate in an Evaluation Kit. The Evaluation Kit will be compatible with common 3rd party development environments used by both DIBs and Commercial customers. This enables these customers to accelerate system level evaluations and designs that can use either a Storefront version of the 12LP Test Chip or our eFPGA Hard IP in an ASIC. We anticipate having Evaluation Kits available in late 2026.

With that, I will turn the call over to Elias for his presentation of financial data.

Elias Nader, CFO

Thank you, Brian and good afternoon, everyone.

Total third quarter revenue was $2.0 million and aligned with the midpoint of our guidance. Total revenue was down 52.5% from Q3 2024 and down 45% compared to Q2 2025.

Rounded to the nearest $100 thousand, new product revenue in Q3 was $1.0 million and mature product revenue was $1.1 million.

New product revenue was down 73.1% from Q3 2024 and down 67.3% compared to Q2 2025. Mature product revenue was up from $0.7 million in the third quarter of 2024 and up from $0.8 million in the second quarter of 2025.

Non-GAAP gross margin in Q3 was a negative 11.9%. This compared with non-GAAP gross margin of 65.3% in Q3 2024 and 31.0% in Q2 2025. The primary reasons for the lower Q3 gross profit margin are unfavorable absorption of fixed costs due to lower revenue and the fact that $300 thousand of R&D costs were allocated to COGs.

Non-GAAP operating expenses in Q3 were approximately $2.9 million. This was approximately $300 thousand below the mid-point of our outlook due to the COGS allocation I just mentioned. This compares with non-GAAP operating expenses of $3.3 million in the third quarter of 2024 and $2.5 million in the second quarter of 2025.

Non-GAAP net loss was $3.2 million, or $0.19 cents per diluted share. This compares to non-GAAP net loss of $0.9 million, or $0.06 per diluted share in Q3 2024, and a non-GAAP net loss of $1.5 million, or $0.09 cents per diluted share, in the second quarter of fiscal 2025.

The difference between our GAAP and non-GAAP results is related to non-cash, stock-based compensation expenses, impairment charges, and restructuring costs. Stock based compensation for Q3 was $0.8 million. Stock

based compensation was $1.2 million in Q3 2024 and $0.8 million in Q2 2025. Impairment charges were $0.3 million in Q2 2025.

For the third quarter, three customers accounted for 10% or more of total revenue.

At the close of Q3, total cash was $17.3 million, inclusive of utilization of $15 million from our $20 million credit facility. This compares with $19.2 million inclusive of usage of $15 million from our $20 million credit facility at the close of Q2 2025.

Net of approximately $200 thousand raised with our ATM in July, cash usage during Q3 was approximately $1.9M. This was primarily driven by tape-out and wafer costs associated with our internally financed SRH FPGA Test Chip. In addition to these one-time costs, there were also expenditures related to revenue contracts and repayments for financed tooling and equipment.

Now moving to our guidance and outlook for our fiscal fourth quarter, which will end on December 28, 2025.

Based on backlog and customer forecasts, we are targeting total revenue of $6 million for Q4.

Many of the contracts that support this outlook are already on the books or have been forecasted by customers to be awarded during the coming weeks. However, the customer for a contract valued at nearly $3 million for a commercial application has forecasted the award late in the quarter.

If this contract is awarded on or very near the date forecasted, we will be able to recognize a large portion of that revenue in Q4, and with that, realize our $6 million objective. We have a very high level of confidence in winning this contract, but note that it could push into Q1 2026, and that would result in Q4 revenue of $3.5 million. Due to this, our guidance range for total Q4 revenue is $3.5 million to $6.0 million.

At $3.5 million, we expect total revenue to be comprised of $2.5 million in new product revenue and $1.0 million in mature product revenue. At $6.0 million, we expect $5 million in new product revenue.

Based on the anticipated Q4 revenue mix, non-GAAP gross margin for the fourth quarter is expected to be approximately 45% at $3.5 million of revenue and 68% at $6.0 million of revenue. At the low end of the range, the primary reason for a lower gross profit margin is attributed to less favorable absorption of fixed costs.

Taking the range of our Q4 outlook into consideration, our full-year 2025 non-GAAP gross profit margin is expected to be 38% plus or minus 5%.

Our Q4 non-GAAP operating expenses are expected to be approximately $3.0 million, plus or minus 5%. With this, we are modeling full year 2025 non-GAAP op/ex will be approximately $11.3 million.

Please note that given the nature of our industry, we may occasionally need to classify certain expenses to COGS versus op/ex or capitalize certain costs. These classifications are related to labor and tooling for our IP contracts with customers. This may cause variability in our quarterly gross margins and operating results that will usually balance out on the operating line.

After interest and other income, at the low end of the revenue range, we forecast a Q4 non-GAAP net loss of approximately $1.9 million or $0.11 per share. At the high end of our revenue range we are projecting a non-GAAP net profit of approximately $600 thousand or $0.04 per share.

The main difference between our GAAP and non-GAAP results is related to non-cash, stock-based compensation expenses. In Q4, we expect this compensation will be approximately $800 thousand. This is the same as Q3 2025 and down slightly from Q4 2024.

As a reminder, there will be movement in our stock-based compensation during the year, and it may vary each quarter based on the timing of grants.

Even at the low end of our revenue guidance range, we anticipate positive cash flow in Q4. However, the timing of payments from our U.S. Government Contract could negatively impact this outlook. Given the fact we raised approximately $2 million using our existing ATM in October, we are well prepared for any delayed payments associated with our U.S. Government Contract.

Thank you.

With that, let me now turn the call over to Brian for his closing remarks.

Brian Faith, CEO

Thank you, Elias.

We have logged considerable progress during the last few months and we are leveraging that progress to produce tangible results. Earlier I talked about those results and now I would like to take the next few minutes to help you understand the industry trends that are driving these results. With that understanding, I think you will appreciate what is driving the increased interest in FPGA technology and why more companies are incorporating larger blocks of eFPGA at the core of new ASIC designs.

The over-arching trend in both Commercial and DIB designs is Smart Systems. Smart Systems rely on algorithms for their intelligence. Algorithms can be processed much faster and with much lower power consumption in hardware than software. Hardware processing is also inherently more secure against cyber threats than software.

The challenge here is that algorithms must be updated over the lifecycle of the product. This means hardware must be programmable so it can adapt to changing algorithms. This has led to the need for larger blocks of eFPGA at the heart of ASIC designs versus past use cases where small blocks of eFPGA were more commonly used as programmable connectivity bridges. This means both the need and the value proposition for eFPGA are increasing.

Sophisticated Smart Systems designs typically target advanced fabrication nodes. This means higher fixed costs and longer design cycles for ASICs.

To favorably offset these higher fixed costs, ASIC designs must deliver longer life-cycles than in the past. Designs that employ eFPGA can adapt to changing algorithms, evolving functional requirements and external changes

that are not evident during the design cycle. This flexibility lengthens the life-cycle of ASIC designs and provides program managers with the confidence to move ASICs to production more quickly and with lower risk. This shortens design cycles and lowers development costs.

Last, but certainly not least, there are many programs in development today that must be compliant with rigorous environmental requirements ranging from Radiation Tolerant to Strategic Rad Hard. Our internally funded development of an SRH FPGA Test Chip is designed to address the full range of these requirements and accelerates our ability to pursue design wins.

By using the same onshore 12LP fabrication process that DIBs have used for SRH ASICs, we are optimizing our chances of winning discrete FPGA designs we can Storefront and contracts for eFPGA Hard IP that customers can incorporate in ASIC designs. Further enhancing our position is the fact customers can execute designs with our Aurora User Tools for both.

The fact this investment by QuickLogic has been received very well by strategic DIBs is underscored by the commitment we have for SRH Dev Kit orders that we anticipate receiving by the end of this month.

Before I turn the call over for Q&A, I want to take a moment to recognize Veterans Day and express my heartfelt gratitude to all those who have served our country. This day has personal meaning for me, as several members of my family have served, and I have deep respect for the sacrifices made by veterans and their families. It’s something we honor at QuickLogic, especially as we develop technologies that contribute to our nation’s defense and security.

Operator, I would now like to open the call for questions.

Closing Remarks

Thanks again for joining us today. Hopefully we will connect with some of you at one of our upcoming events including the Craig Hallum Alpha Select 1on1 Conference in New York on November 18th, the semiconductor focused Annual NYC Summit, also in New York, on December 16th or the Annual Needham Growth Conference in early January.

Thank you and have a good day!

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