Q1 Fiscal 2026 Earnings Conference Call Prepared Remarks

Operator

Ladies and gentlemen, good afternoon.
At this time, I would like to welcome everyone to QuickLogic Corporation's First Quarter Fiscal 2026 Earnings Results Conference Call. As a reminder, today's call is being recorded for replay purposes. I would now like to turn the conference over to Ms. Alison Ziegler of Darrow Associates. Ms. Ziegler, please proceed.

Alison Ziegler

Thank you, Cheri, and thanks to all of you for joining us. Our speakers today are Brian Faith, President and Chief Executive Officer, and Elias Nader, Senior Vice President, and Chief Financial Officer.

As a reminder, some of the comments QuickLogic makes today are forward-looking statements that involve risks and uncertainties, including but not limited to statements regarding our future profitability and cash flows, expectations regarding our future business and statements regarding the timing, milestones, and payments related to our government contracts, statements regarding the expected magnitude of potential contracts, and statements regarding expected adoption rates and/or orders by our customers

Actual results may differ due to a variety of factors including: delays in the market acceptance of the Company's new products; the ability to convert design opportunities into customer revenue; our ability to replace revenue from end-of-life products; the level and timing of customer design activity; the market acceptance of our customers' products; the risk that new orders may not result in future revenue; our ability to introduce and produce new products based on advanced wafer technology on a timely basis; our ability to adequately market the low power, competitive pricing and short time-to-market of our new products; intense competition by competitors; our ability to hire and retain qualified personnel; changes in product demand or supply; general economic conditions; political events, international trade disputes, natural disasters and other business interruptions that could disrupt supply or delivery of, or demand for, the Company's products; and changes in tax rates and exposure to additional tax liabilities.

For more detailed discussions of the risks, uncertainties and assumptions that could result in those differences, please refer to the risk factors discussed in QuickLogic's most recently filed periodic reports with the SEC. QuickLogic assumes no obligation to update any forward-looking statements or information, which speak as of the respective dates of any new information or future events.

In today's call, we will be reporting non-GAAP financial measures. You may refer to the earnings release we issued today for a detailed reconciliation of our GAAP to non-GAAP results and other financial statements. We have also posted an updated financial table on our IR web page that provides current and historical non-GAAP data.

Please note, QuickLogic uses its website, the company blog, corporate Twitter account, Facebook page, and LinkedIn page as channels of distribution of information about its business. Such information may be deemed material information, and QuickLogic may use these channels to comply with its disclosure obligations under Regulation FD.

A copy of the prepared remarks made on today's call will be posted on QuickLogic's IR web page shortly after the conclusion of today's earnings call.

I would now like to turn the call over to Brian.

Brian Faith: CEO

Thank you Alison, Good afternoon everyone, and thank you all for joining our first quarter 2026 conference call.

Since our last conference call, we have made significant progress towards our goal of delivering 50% to 100% year-over-year revenue growth in 2026. With this, we continue to expect Storefront and our new RadPro™ FPGA will contribute to our anticipated revenue growth and second half profitability.

As we announced in an April 9th press release, we introduced and demonstrated our new RadPro FPGA and Development Kit at the Hardened Electronics and Radiation Technology or HEART Conference last month. HEART is a highly specialized conference where attendees

must show proof of U.S. Citizenship and their affiliation with a company or academia that is certified through the Joint Certification Program.

RadPro is our trademarked brand for radiation-hardened FPGAs. The Test Chip we demonstrated at the HEART Conference with our RadPro Dev Kit was internally funded and is independent of our U.S. Government contract. These Test Chips were fabricated on the GlobalFoundries 12LP process, which is the same process used by many DIBs for radiation hardened ASICs.

This means that in addition to successfully demonstrating our new discrete RadPro FPGA, we have also illustrated our capability to support requirements for eFPGA in radiation-hardened ASICs and SoCs fabricated on the GlobalFoundries 12LP process.

Our demonstrations and meetings at HEART with leading DIBs went very well, and we have since shipped multiple RadPro Dev Kits. These shipments will provide a low-six-figure contribution to our Q2 revenue.

While we expect it will take until the end of 2026 for DIBs to fully evaluate our new RadPro FPGA, we have already signed an MOU with one DIB to accelerate the mutual evaluation of a potential RadPro chiplet application.

In addition to the progress we've made with our RadPro FPGA, in a March 17th press release, we announced our fourth contract targeting Intel 18A technology. While these initial contracts have been smaller, their total value is now nearly $2 million and together they are the framework for the larger contracts we expect to book later this year.

The first two contracts were for Intel 18A Test Chips. We anticipate receiving our Test Chip allocation from the first contract later this quarter. We believe the data we gather from our evaluation of these Test Chips will enhance our ability to win new production contracts.

The third contract was for a one-million LUT feasibility study, which led us to implement some notable architectural enhancements that we can leverage across all advanced fabrication nodes.

With these architectural enhancements in place, we can address the lucrative markets that require very high-density eFPGA cores in ASIC designs and very high-density discrete FPGAs. This significantly expands our SAM for eFPGA Hard IP and discrete devices, including chiplets and a variety of Storefront opportunities.

The fourth, and most recent contract leverages the architectural enhancements that were developed during the one-million LUT feasibility study. In support of this contract, we will deliver Hard IP for a very large Intel 18A eFPGA core in support of our customer's ASIC design. The Test Chip for this ASIC design is targeted for tape-out during the second half of 2026. We anticipate a fifth mid-six-figure contract from this customer during the second half of 2026 that further extends our work on very high-density architecture.

While the timing of funding remains uncertain, our discussions with this DIB have expanded to include the potential of QuickLogic providing Storefront services for a customer-designed ASIC that will include our eFPGA Hard IP. We expect to learn more about the potential expansion to Storefront services and the timing of this possible award in the coming months.

In addition to these DIB contracts, we are working closely with a large commercial customer contract based on Intel 18A valued at several million dollars. In our last conference call, I said that I expected this contract would be awarded in late Q2. However, the customer is evaluating an expansion in the size and function of the eFPGA core in their ASIC to provide greater programmable flexibility. While this is a beneficial trend for QuickLogic, we are now forecasting this contract to be awarded during Q3.

On December 8th we issued a press release announcing Idaho Scientific selected our eFPGA Hard IP for forward-leaning, hardware based cryptographic solutions designed to address Mobile, IoT, Infrastructure and Defense Systems applications. We are continuing to support the integration of our Hard IP into the tape-out that is anticipated next year.

Idaho Scientific has a rich history in leveraging FPGA technology to deliver robust security systems that can adapt quickly to changing external threats without the vulnerabilities that are inherent in software-based solutions. By integrating our eFPGA Hard IP into its Secure System on a Chip processors, Idaho Scientific can further enhance its cryptographic security and address new markets much more quickly with lower risks and lower costs.

Since our last conference call, Idaho Scientific has been fully integrated with General Dynamics Mission Systems. We believe this integration may lead to new opportunities for QuickLogic.

Last year we announced an eFPGA Hard IP contract with a new Defense Industrial Base customer valued at $1.1 million that will be fabricated on the GF 12LP process. This application utilizes a large block of our eFPGA Hard IP for critical functions, which is a trend we are seeing in designs targeting advanced fabrication nodes.

With the cooperation of this DIB and its end-customer, we have leveraged the large eFPGA core to win a new seven-figure contract that was finalized last week and will contribute to Q2 revenue. The delay of this award is why our Q1 revenue was below the midpoint of our guidance.

In the scope of this new contract, we will be provided with Test Chips that we will incorporate in an Evaluation Kit. The Evaluation Kit, which is currently scheduled for late 2026, will be compatible with common 3rd party development environments used by both DIBs and Commercial customers. This enables these customers to accelerate system level evaluations and designs that can use either a Storefront version of the discrete FPGA or our eFPGA Hard IP in an ASIC.

In parallel with these efforts, we're exploring the potential to leverage the FPGA from this contract as a Storefront Chiplet. We are already seeing interest from some of our partners on this concept.

Due largely to the strategic initiatives we launched in 2025, we believe we are building meaningful traction in the Chiplet markets. We are currently working on numerous proposals at various stages that include direct U.S. Government, DIB and commercial applications. These proposals include opportunities targeting several fabrication processes including GlobalFoundries 12LP and Intel 18A.

Last year, the commercial chiplet ecosystem was mired in debate regarding the communications and protocol layers. In response, we introduced the first phase of our

Digital Proof of Concept Chiplet program as a strategy to move forward prior to customer commitments and with that, accelerate our Storefront Chiplet initiative.

Internally, we refer to this as POC. With the support of our large strategic partners, we leveraged our existing eFPGA Hard IP and readily available 3rd party IP to move this program forward rapidly and with minimal investment.

We presented a paper on the POC at Chiplet Summit in mid-February and gave a presentation with Intel Foundry at an event at the Government Microcircuit Applications & Critical Technology or GOMACTech Conference in March. As a reminder, QuickLogic is a member of the Intel Foundry Accelerator Ecosystem Alliance program, participating in the Chiplet, IP and USMAG Alliances.

In our last conference call, I stated that the net takeaway from our presentation at the Chiplet Summit supports our optimism that Chiplets will build traction in 2026. This opinion was bolstered at the GOMACTech conference. The primary hurdles today are interoperability gaps, and we believe a Storefront FPGA Chiplet is the logical solution for a programmable bridge.

With that, I will turn the call over to Elias for his presentation of financial data.

Elias Nader, CFO

Thank you, Brian and good afternoon everyone.

Total first quarter revenue was $5.1 million. This was up 16.5% from Q1 2025 and up 35.3% from Q4 2025. Revenue was approximately $450 Thousand below the midpoint of our guidance due to a delay in the award of a certain contract that we finalized last week.

Revenue recognition for this contract will be ratable and will now extend through Q1 2027 versus through Q4 2026. This shift forward in revenue recognition does not impact the full year revenue outlook that Brian shared earlier.

New product revenue in Q1 was $4.3 million and mature product revenue was $0.8 million.

New product revenue was up 14.2% from Q1 2025 and up 50.7% compared to Q4 2025. Mature product revenue was up 31.7% compared to the first quarter of 2025 and down 14.2% from the fourth quarter of 2025.

Non-GAAP gross margin in Q1 was 39.6%. This was below our outlook of 45% plus or minus 5%. The shortfall was primarily due to inventory reserves of $298 thousand. This compares to 45.7% in Q1 2025 and 20.8% in Q4 2025.

Non-GAAP operating expenses in Q1 were approximately $3.3 million. This compares to $3 million in Q1 2025 and $3.5 million in Q4 2025.

Q1 2026 Non-GAAP net loss was $1.3 million, or a loss of $0.08 per share. This compares to a non-GAAP net loss of $1.1 million, or a loss of $0.07 per share in Q1 2025, and a non-GAAP net loss of $2.8 million, or a loss of $0.17 cents per share, in the fourth quarter of fiscal 2025.

The difference between our GAAP and non-GAAP results is primarily related to non-cash stock-based compensation expenses. Stock based compensation for Q1 was $858 thousand compared to $904 thousand in Q1 2025 and $744 thousand in Q4 2025. Restructuring costs were $11 thousand in Q1 2026, compared with $141 thousand in Q1 2025 and $0 in Q4 2025.

For the first quarter, two customers accounted for 10% or more of total revenue.

At the close of Q1, net cash was $6 million. This compares with $3.8 million in net cash at the close of Q4 2025. This increase of $2.2 million in net cash is inclusive of $3.2 million raised with our ATM during Q1-2026.

Now moving to our guidance and outlook for our second fiscal quarter, which will end on June 28, 2026.

Based on backlog and customer forecasts, our total revenue guidance for Q2 is $6.0 million plus or minus 10%.

We expect total revenue to be comprised of $5.2 million in new product revenue and $0.8 million in mature product revenue. We anticipate an increase in mature product revenue during the second half that drives the full year total to approximately $4 million.

Based on the anticipated Q2 revenue mix, non-GAAP gross margin for the second quarter is expected to be approximately 42% plus or minus 5%. As I noted in our last conference call, there are several factors weighing on our non-GAAP gross profit margin during the first half of 2026. For the full year, we are still modeling a non-GAAP gross profit margin of approximately 57%.

Please note that given the nature of our industry, we may occasionally need to classify certain expenses to COGS versus op/ex or capitalize certain costs. These classifications are related to labor and tooling for our IP contracts. This may cause variability in our quarterly gross margins and operating expenses that will usually balance out on the operating line.

With that in mind, our Q2 non-GAAP operating expenses are expected to be approximately $3.3 million plus or minus 5%. We are still expecting full year non-GAAP operating expenses to be approximately $13.5 million. This forecasted growth of approximately 14% in non-GAAP op/ex over 2025 is to support our anticipated 50% to 100% revenue growth in 2026 that Brian mentioned earlier.

After interest and other income, we are forecasting a Q2 net loss of about $800 thousand or a loss of approximately $0.04 per share. Based on our current outlook, we anticipate non-GAAP profitability for the second half of 2026.

The main difference between our GAAP and non-GAAP results is related to non-cash, stock-based compensation expenses. In Q2, we expect this compensation will be approximately $900 thousand, which is similar to Q1 2026 and Q2 2025.

As a reminder, there will be movement in our stock-based compensation during the year, and it may vary quarter to quarter based on the timing of grants.

We raised approximately $6.4 million in Net Proceeds during Q2-2026 using our existing ATM. Based on our current outlook, we do not anticipate further sales using our existing ATM during the balance of fiscal year 2026.

Excluding money raised with our ATM, we anticipate Q2 cash use of approximately $500 thousand. Inclusive of money raised with our ATM, we anticipate closing Q2 with just under $12 million in net cash.

Please note that our cash use could vary based on the timing of certain payments and receipts from contracts during the quarter. Based on our current outlook, we anticipate positive cash flow during the second half of 2026.

As reported in our 8K filed on April 30, 2026, we have secured a new banking partner. With this new agreement, and considering the amount we have raised with our ATM, we intentionally lowered our credit line to $10 million and secured more favorable terms that will lower our borrowing costs.

Thank you for your time, and with that, I will now turn the call over to Brian for his closing comments.

Summation:

The entire QuickLogic team has worked very hard to accomplish numerous tangible milestones that have set the stage well for 2026 and beyond. This execution, along with Strategic Investments and Strong Customer Alliances are the driving forces for the revenue growth we are forecasting to begin this year.

The most significant investments have been our development of eFPGA Hard IP for Intel 18A technology, and the tape-out of our first RadPro FPGA Test Chip. These internally funded investments have provided us with unique positioning in the market and have enabled us to develop close alliances with strategic customers that we believe will benefit QuickLogic for years to come.

With our first RadPro FPGA in hand, we have already received numerous orders for our RadPro Dev Kits for evaluation. Shipment of these Dev Kits will make a low six-figure contribution to our Q2 revenue. This positions us very well to address applications for various levels of Radiation Hardened discrete FPGAs and eFPGA Hard IP for customer ASIC and SoC designs.

Our early investments to become the first, and as it stands today, only company to offer eFPGA Hard IP for Intel 18A has also enabled us to build strong customer alliances.

One of these customers has already awarded us four contracts with a fifth anticipated during the second half of 2026. Through these contracts we expect to receive our allotment of Test Chips that will enable us to fully characterize the performance of our eFPGA Hard IP on Intel 18A. With these data in hand, I believe we can accelerate new contract awards for DIB and Commercial applications.

This customer also funded the one-million LUT on Intel 18A feasibility study that led us to implement a number of architectural enhancements. These enhancements have expanded our SAM to include the lucrative markets for very high-density discrete FPGAs and eFPGA Hard IP blocks in ASIC and SoC designs.

In addition to the many initiatives I've outlined today that are designed to power our long-term growth, we are planning three Multi-project wafer or MPW tape-outs this year. All three tape outs are for chips that we intend to sell via our Storefront program.

And I as mentioned earlier, the costs for two of these tape outs will be fully covered by customer contracts that are already on the books. We believe the third tape out will be covered at least in part by a customer contract.

Our strong outlook for 2026 is based largely on the foundation we built during the preceding years. As I hope we have articulated well during this call, the QuickLogic team is intensely focused on the continued execution of the strategic milestones that we believe will fuel our growth and profitability for years to come.

With that, we will now open the call for questions.