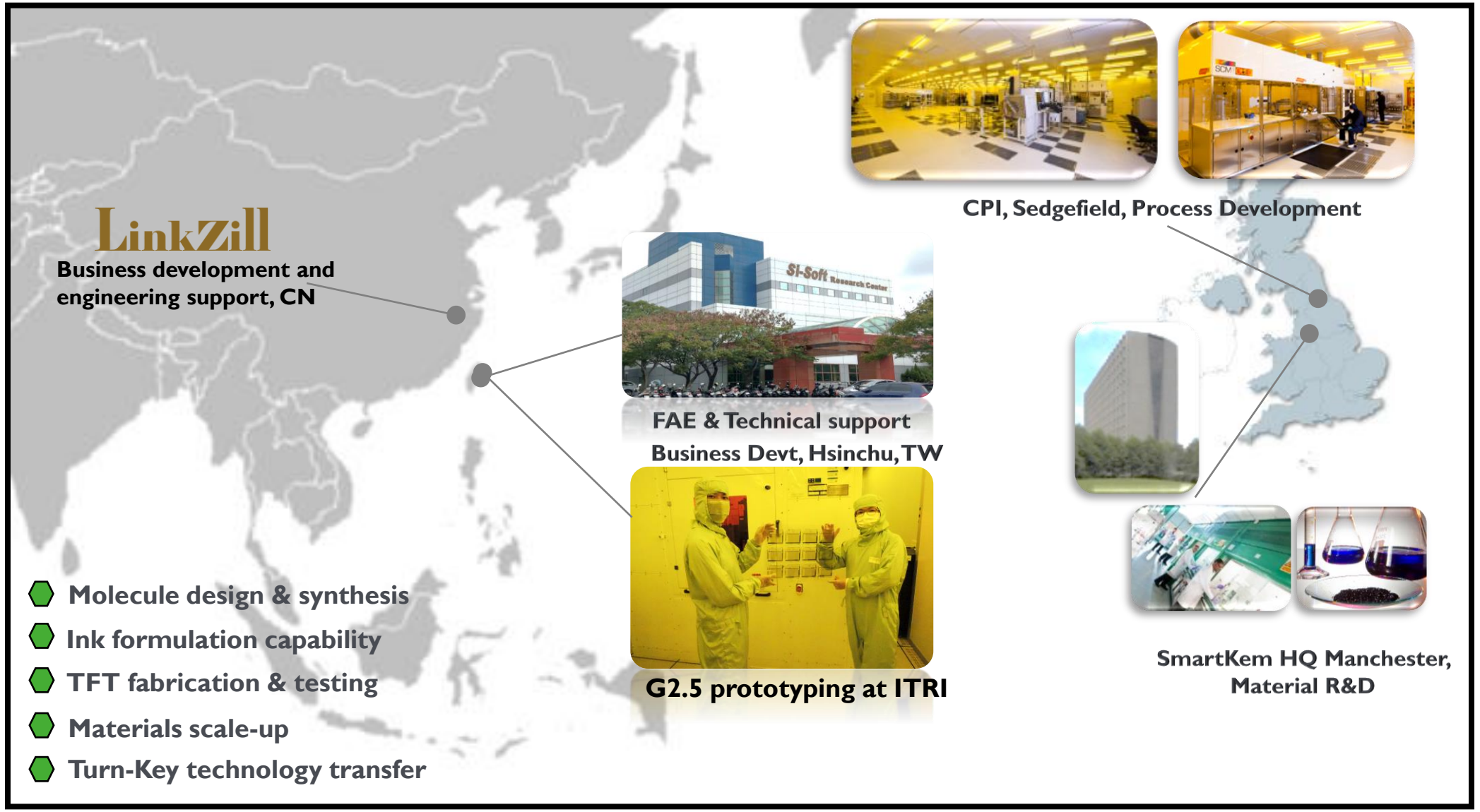
Smartkem

Simon Ogier – (CTO) Smartkem (25th April 2024)

Organic Thin-Film Transistor Technology – from Lab to Fab

Facilities in UK and Asia



Smartkem Facilities: UK & Asia

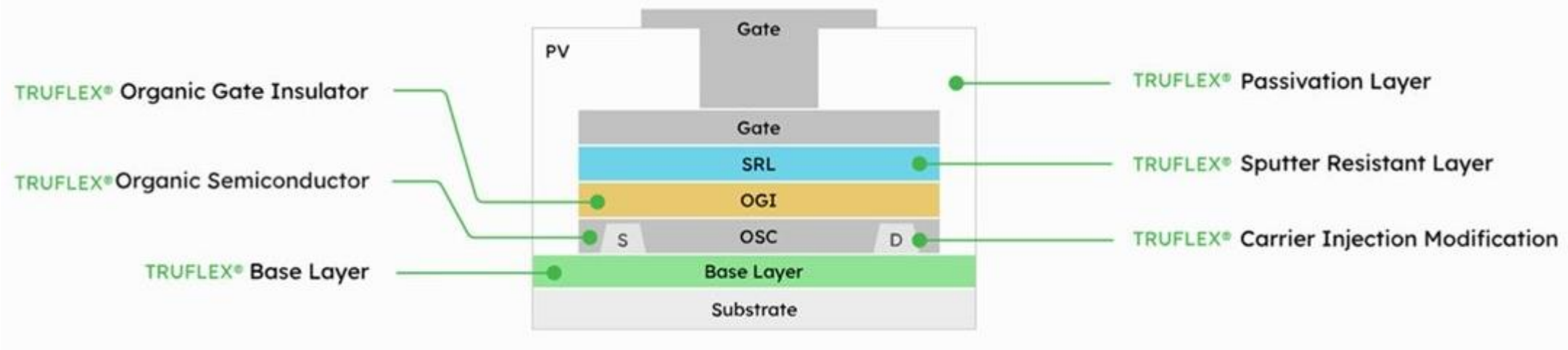
CPI, Sedgefield
Process Development

Smartkem HQ, Manchester
Material research & development

LinkZill, China
Business Development and engineering support

FAE Office, Taiwan
Business development & technical support

Smartkem's TRUFLEX® Materials



All organic materials supplied for tech. transfer

Chemistry, device design and processing guidance provided

Solution processed, process temp as low as 80°C

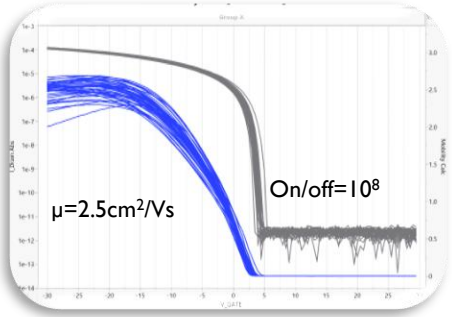
Formed on low-cost glass & plastic

Drop in technology for today's fab lines

Simple, solution-based process

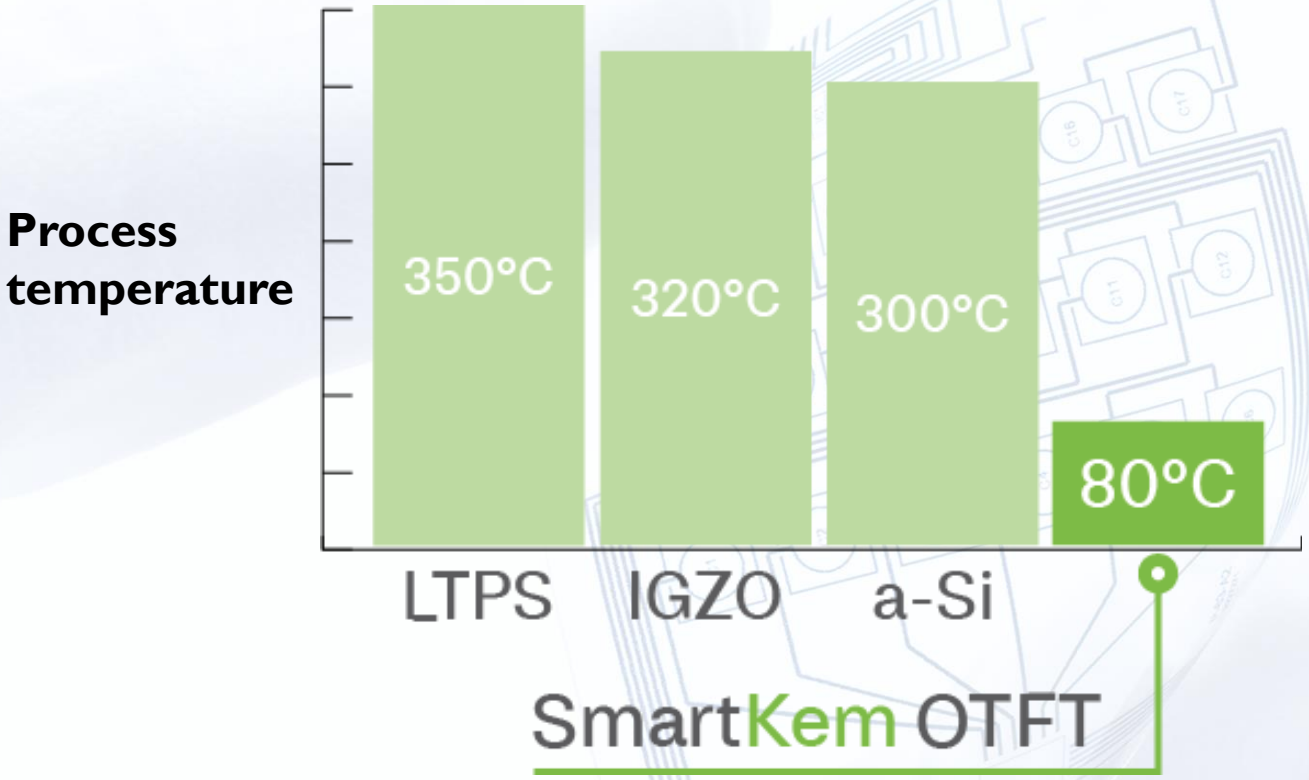
World leading electronic performance

Meets industry critical test standards



Minimal capital re-investment required to adopt on existing a-Si lines

Low temperature Organic Thin-Film Transistor (OTFT) process

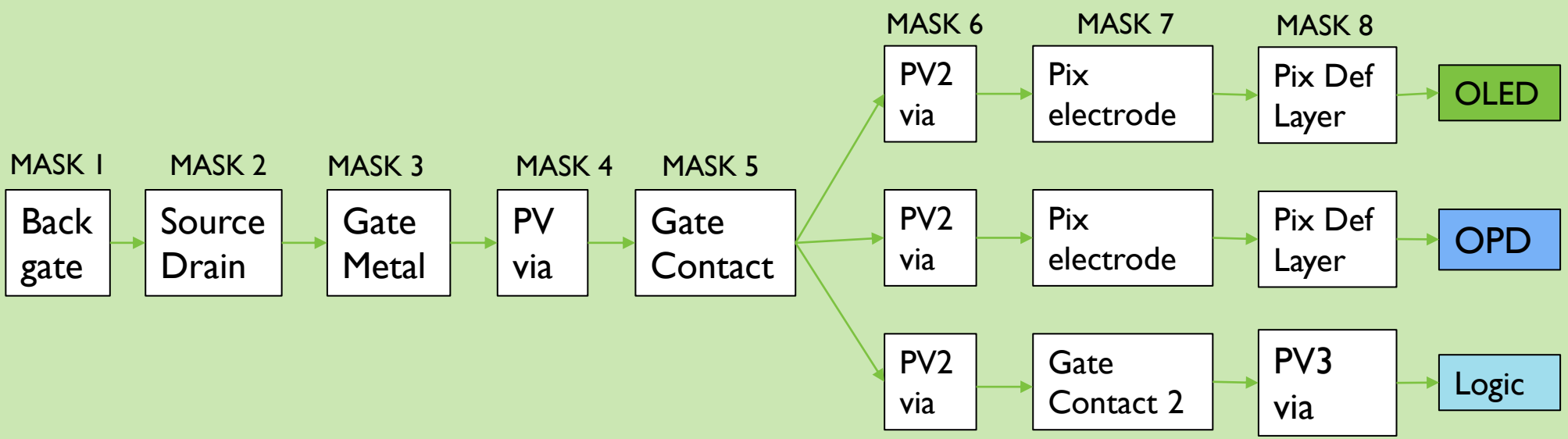


A manufacturing process compatible with amorphous silicon infrastructure and with higher performance

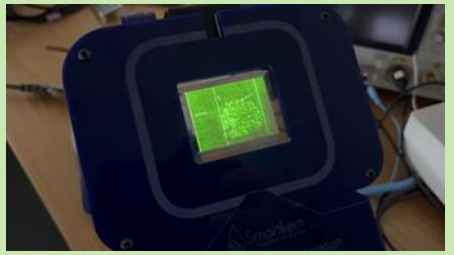
+

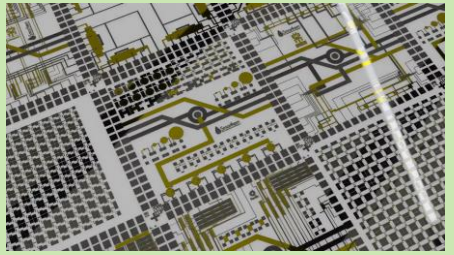
Low temperature processing that enables **backplanes** that are solution-coated on low-cost substrates

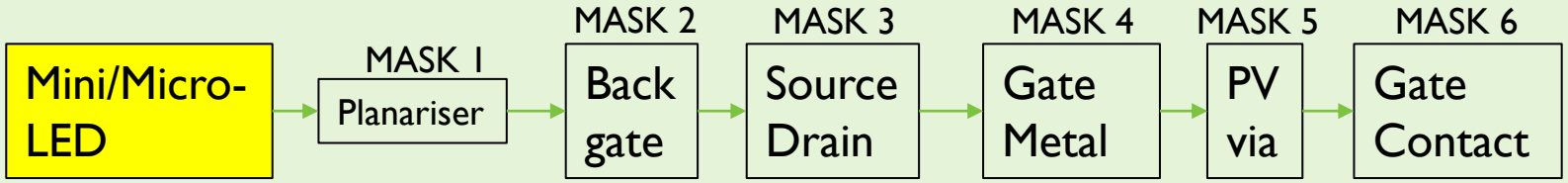
Process flow for OTFT Displays and Circuits

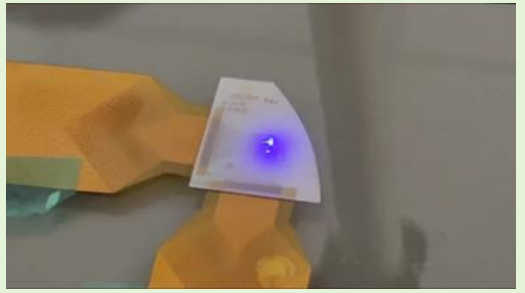


200ppi QVGA AMOLED









254ppi 48x48 OTFT-uLED (0.27” diagonal)

- Logic cells require 5 masks for fabrication (similar process flow as for OLED, OPD, microLED)
- Additional layers PV2/GC2/etc can be used for integration of OLED, OPD, wiring layers
- Capability in OTFT circuitry has been developed in parallel with display activities
  - It is not yet fully enough characterised to offer as a commercial foundry service
  - Digital lithography capability makes OTFT circuitry a low-cost R&D activity

25ppi 27x48 OTFT-mini LED Backlight (2.17” diagonal)

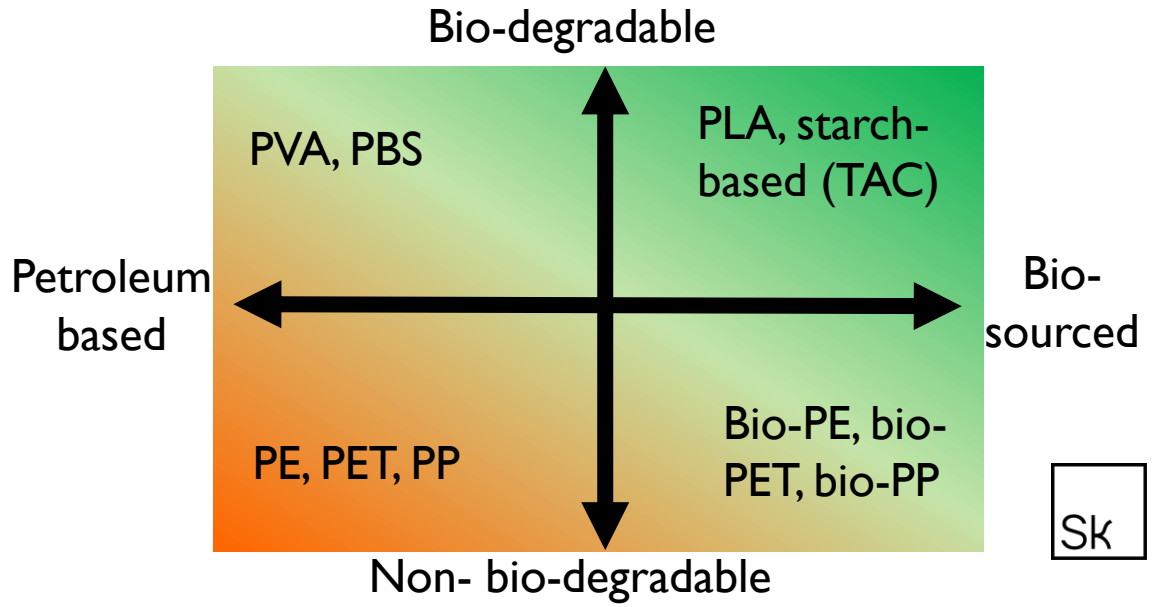
Benefits of low temperature TFT process

1. Energy use - Overall lower energy use in manufacturing (no PECVD)

2. Substrate type - wider choice of plastics with improved properties
   1. Transparency
   2. Biodegradability (<12 months)
   3. Bio-derived (e.g. cellulose)
   4. Low-cost

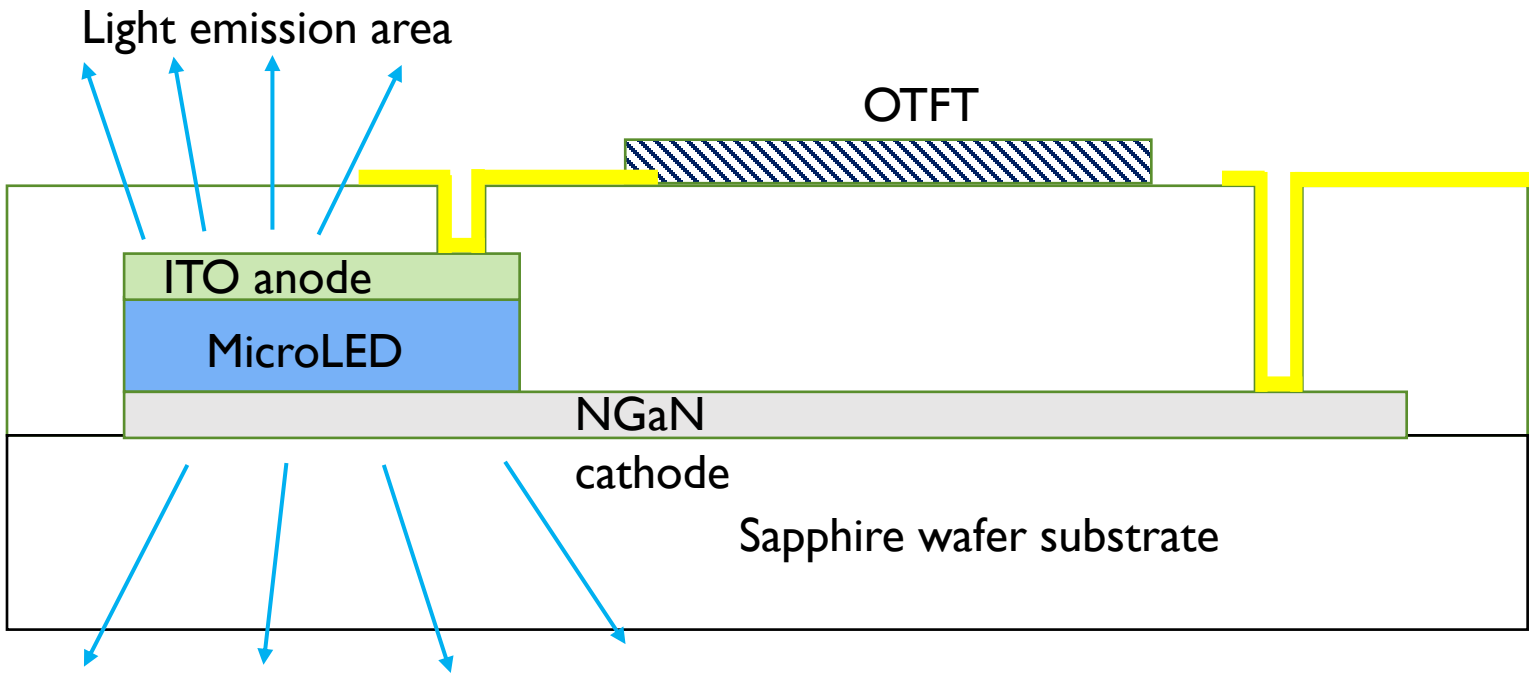
3. Integration benefits - TFT backplane could be processed on top of the device (OLED, micro-LED, etc), potential for R2R manufacturing

Plastic electronics should not add to the plastic waste problem



OTFT µ-led Monolithic Integration

- Integrate OTFT backplane on top of u-LED array on Sapphire or Silicon wafer
- Monolithic integration means no transfer losses



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Wafer-scale organic-on-III-V monolithic heterogeneous integration for active-matrix micro-LED displays

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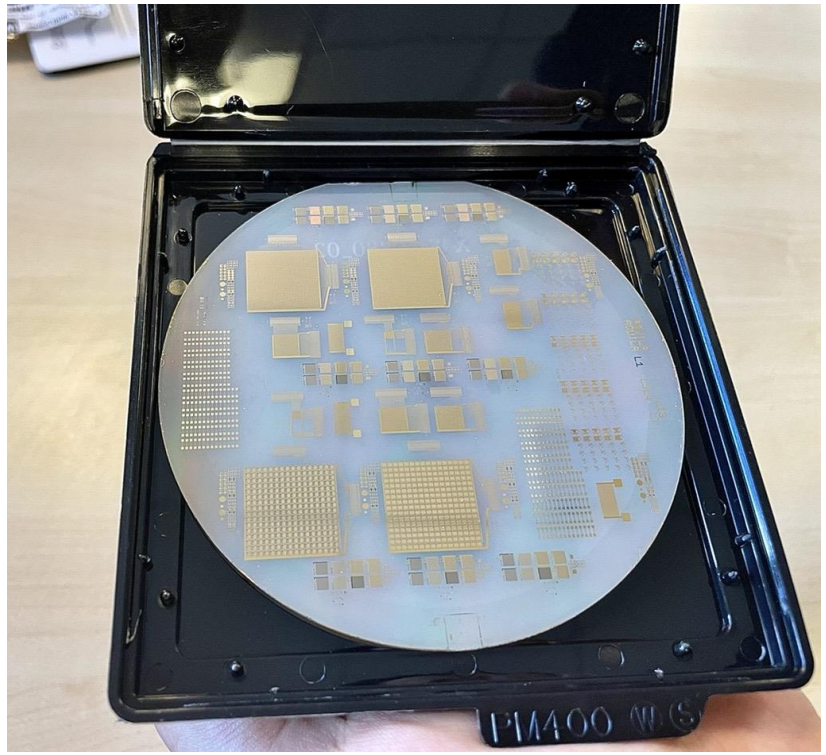
https://www.nature.com/articles/s41467-023-42443-8

In collaboration with SJTU



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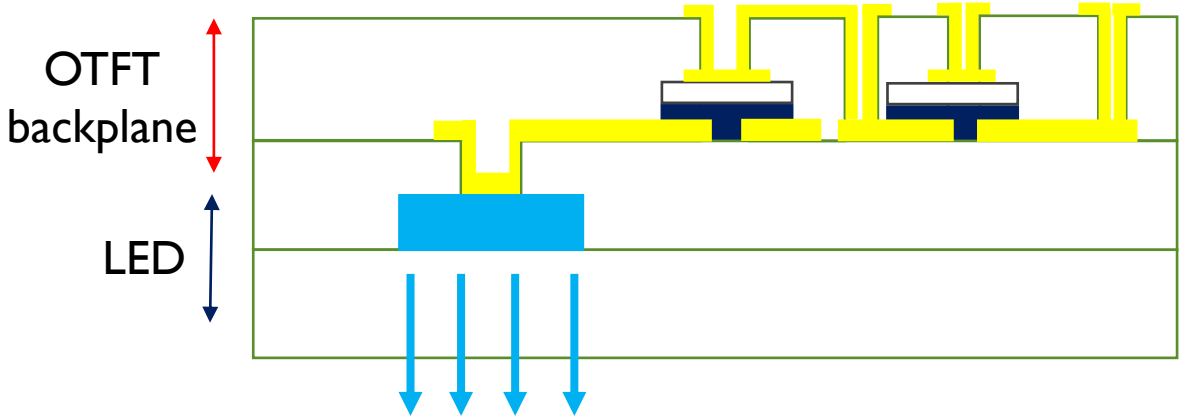
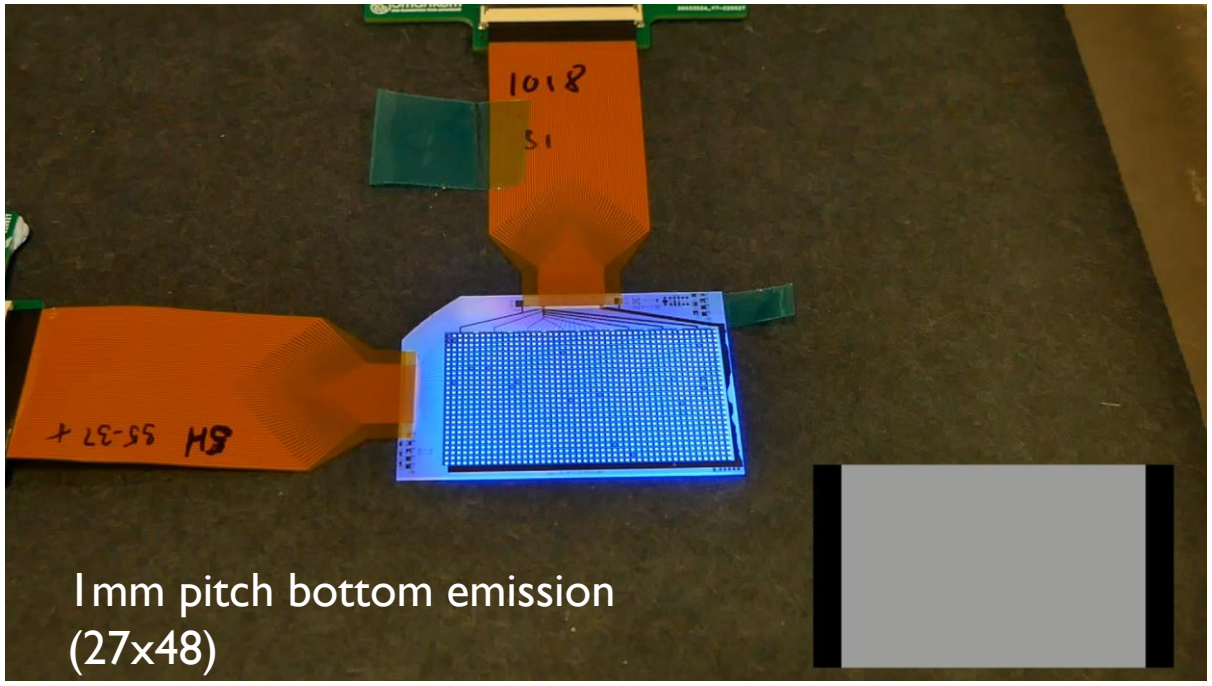
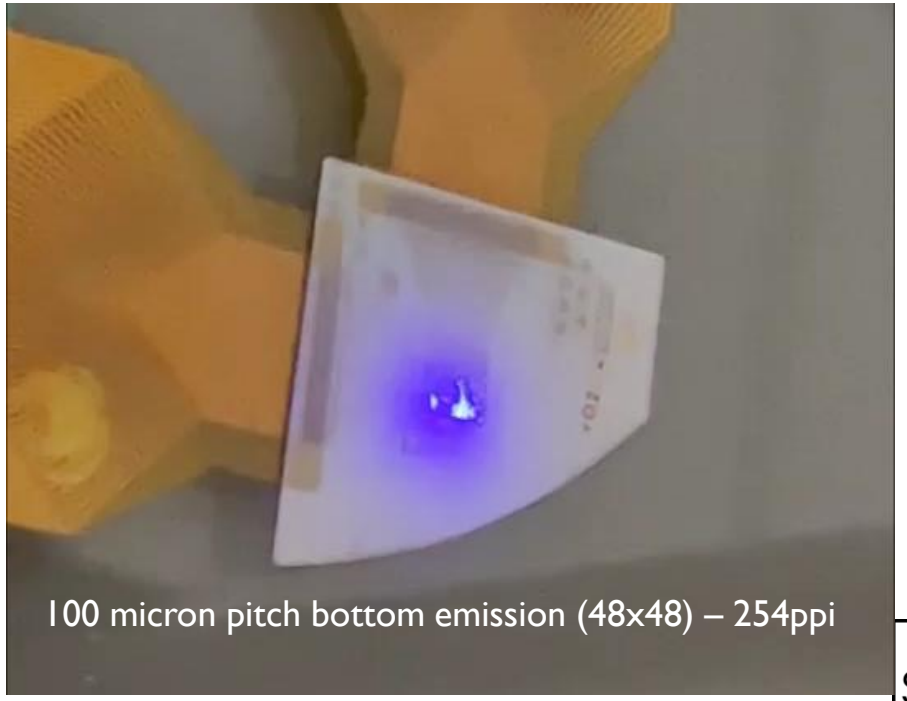
Monolithically Integrated OTFT on MicroLED

- Proof of concept design developed to show how OTFT can be processed on top of u-LED (**no transfer so no transfer yield loss**)
- Initial demos tested to **>100K nits**. Future potential for **>500K** nits with optimised design
- Process can be scaled from **10ppi to >1000ppi** with appropriate lithography tools
- Colour can be integrated through the use of quantum dot colour conversion materials (printed or photopatterned)







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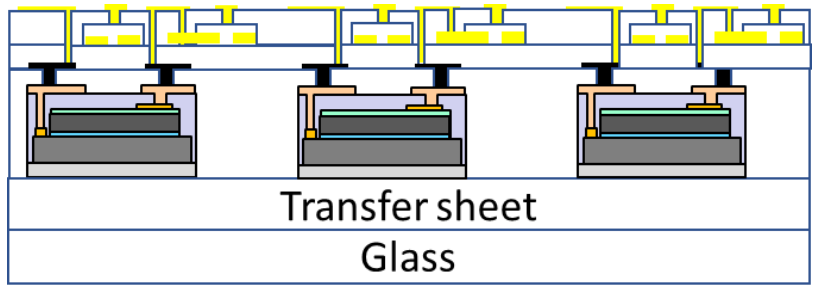
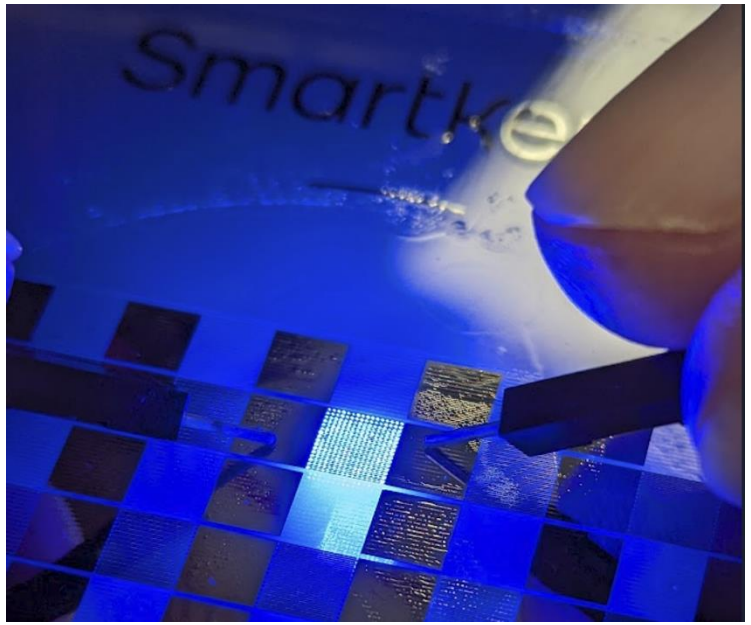
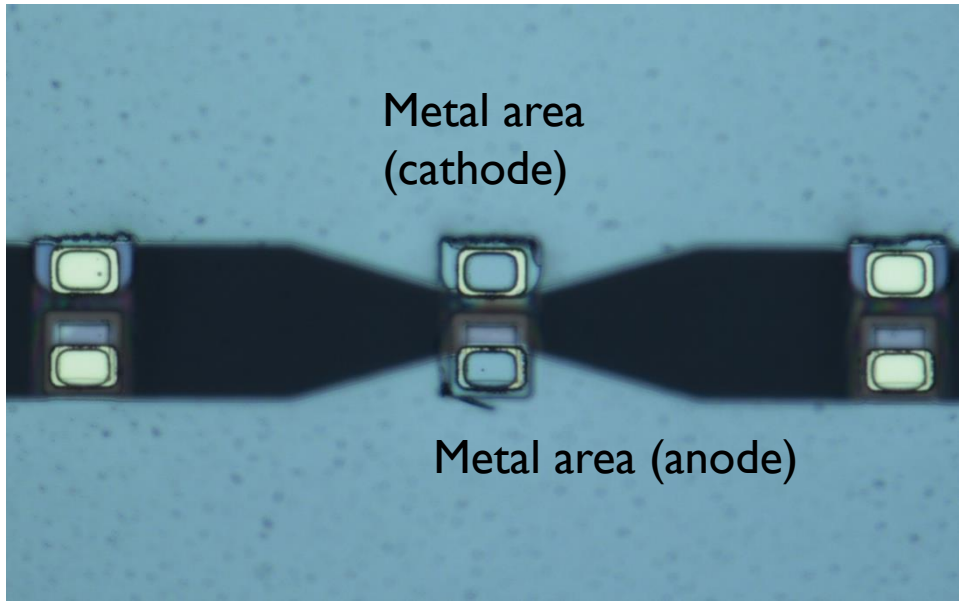
Chip-first Micro-LED Process Development

- GaN cost reduction vs monolithic wafer approach, but some LED transfer costs
- Process trials ongoing to demonstrate our concept of placing micro-LEDs "pads-up", planarising and forming via contacts through the planariser to the LEDs
- Success achieved with direct driving of 110 x 60um LEDs and 20x35um LEDs
- Next step is to form an OTFT backplane on top of the via contacted LEDs (in a similar way to the monolithic micro-LED process demonstrated last year)





20umx35um array of micro-LEDs wired up "chip-first"



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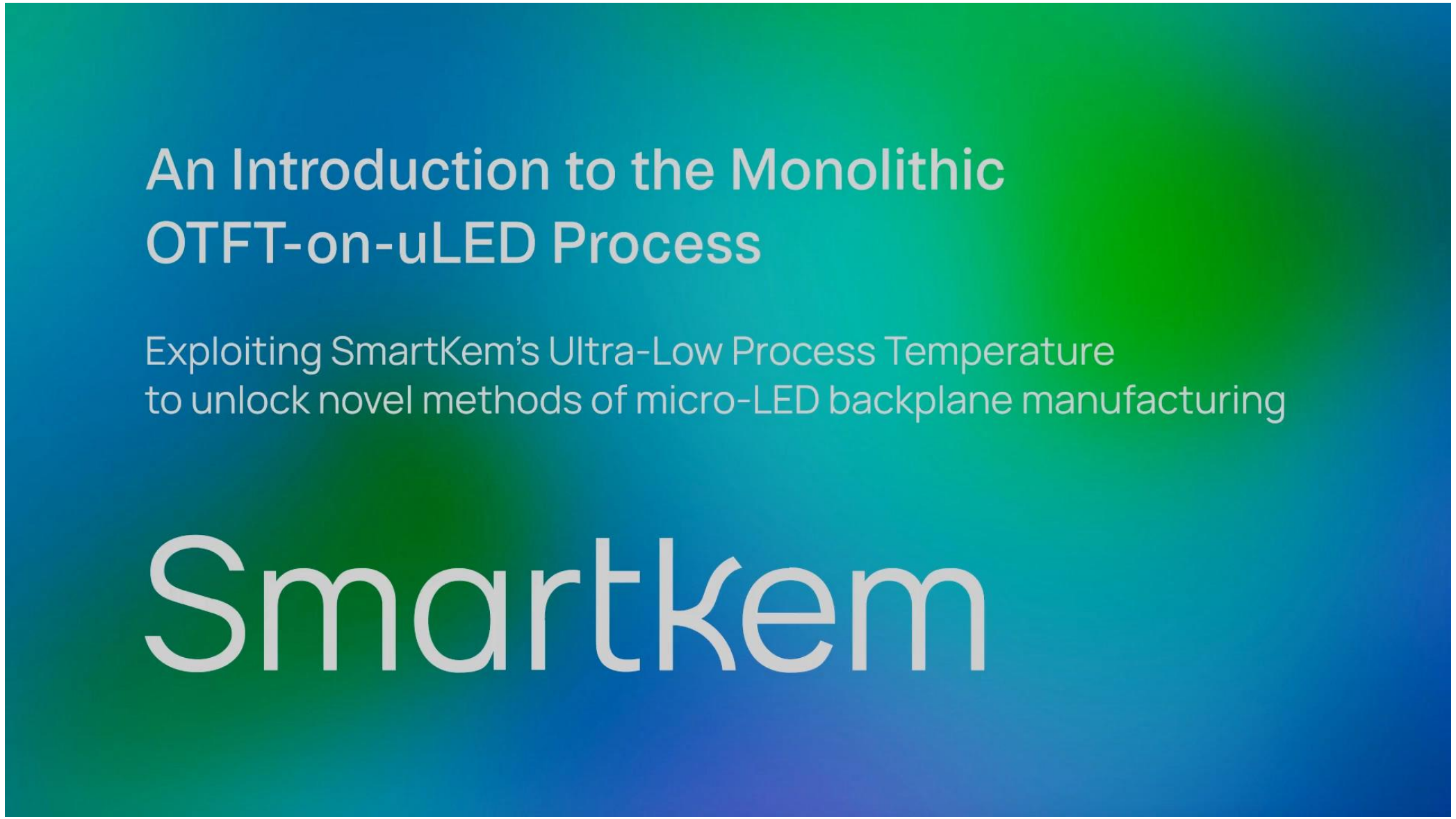
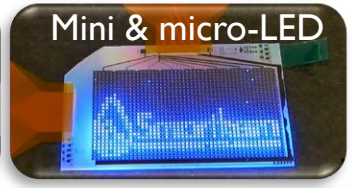
Cost reduction – wafer-based to chip first micro-LED process



Lab to Fab Transition for OTFT products

Stage 1 - 4” or 8” scale
Feasibility and innovation

- Digital lithography employed (fast iteration, low cost)
- Key learnings made (design, performance, application “fit” for technology)
- Design for manufacture (process, materials, equipment)
- Proof of concept stage (small functional display or circuit)

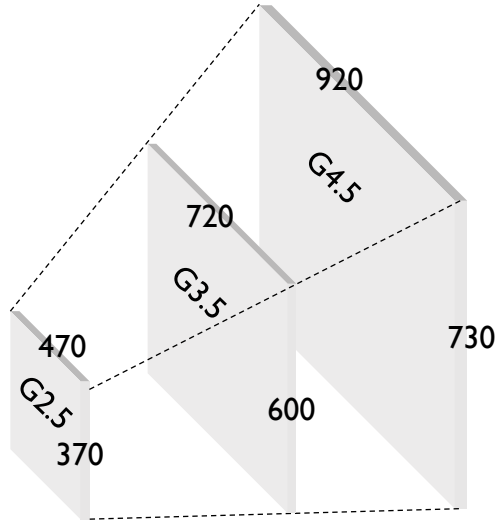


Stage 2 - Gen 2.5 scale
Pilot development

- Process adaptation to industry standard toolset
- Defectivity reduced for displays
- Pilot products used for end user trials
- Product reliability tests
- PDK’s developed for devices

Stage 3
Manufacturing scale-up

- Gen 2.5 or larger
- Technology transfer to display companies
- Manufacturing scale up for new display formats
- Process stabilisation
- New product introduction to market



R&D → Pilot → Manufacturing

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Thank you

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