

Smartkem

Low Warpage Solution for MicroLED Displays



Outline

- About Smartkem Ltd
- The needs for MicroLED displays and their approaches
- An alternative to integrating frontplane and backplane
- Our offerings for display product structure

Presentation to: audience at Touch Taiwan 2024

From: Steven Tsai on 25th Apr 2024





SmartKem Officers



Ian Jenks
Chairman and Chief Executive Officer

Ian was formerly the president of Uniphase Inc, Chairman of Oplink Communications Inc which he took public on the NASDAQ and spent seven years as a partner of Crescendo Ventures llp Ian has been a director of Techstep ASA, Paysafe plc., and Brady plc.



Barbra Keck
Chief Financial Officer

Barbra served as the Chief Financial Officer of Deverra Therapeutics, Inc., a developer of cell therapies. She held positions of increasing responsibility at Delcath Systems, Inc., an interventional oncology company, starting as Controller and ultimately becoming a senior vice president in March 2015 and chief financial officer in February 2017.



Dr. Beverley Brown
Chief Scientist

Beverley has worked in R&D at Imperial Chemical Industries Ltd. ("ICI"), Zeneca Group PLC and at the Avecia Group PLC. Beverley has worked in the field of organic semiconductor technology and in printable electronics for almost 20 years.



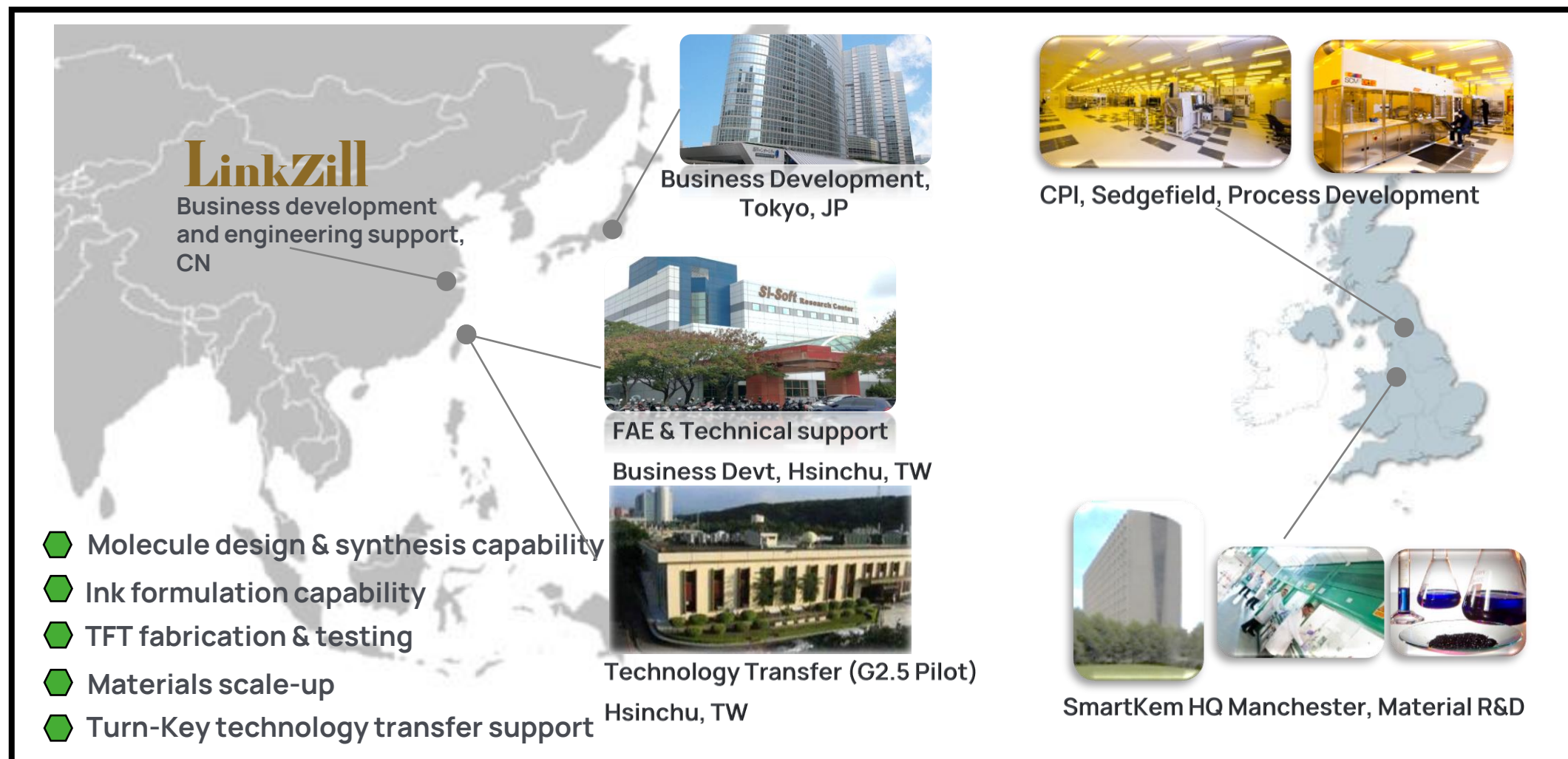
Dr. Simon Ogier
Chief Technology Officer

Simon has previously worked at Avecia, Merck, CPI and more NeuDrive Limited. He currently manages a team of 19 engineers and scientists using the equipment for SmartKem's process development and prototype fabrication. Simon has co-authored 30 journal articles and has been co-inventor on 16 patent families.

History of Smartkem

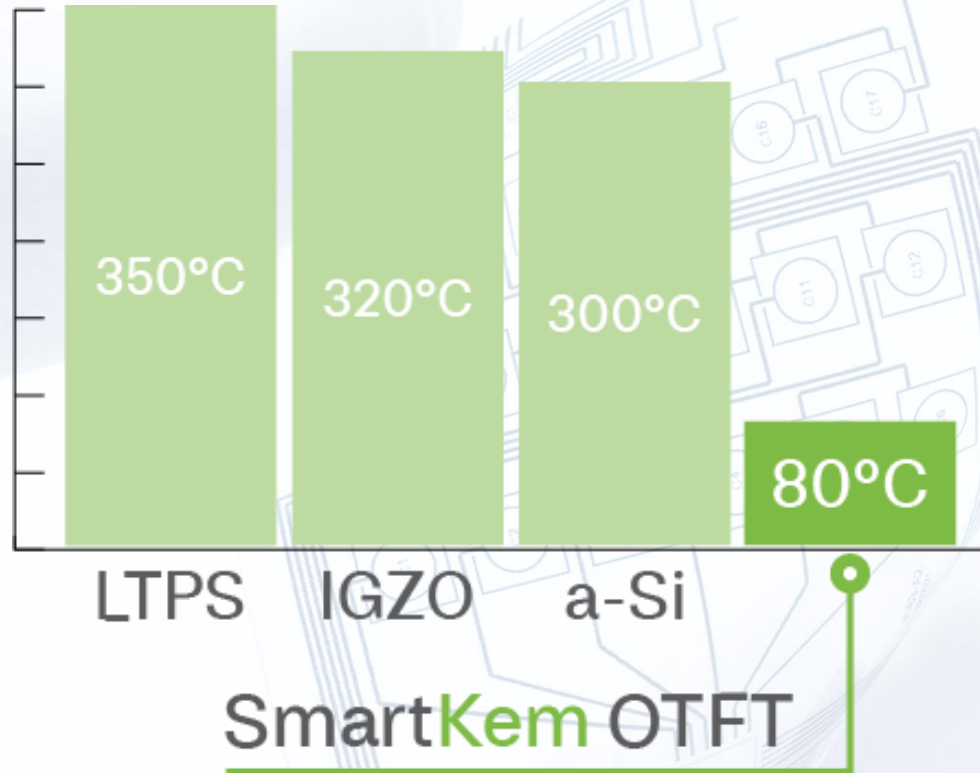
- Established 2009.
- In February 2021, SmartKem raised \$24.6 million in gross proceeds through a private placement of common stock-only at \$2.00 per share.
- To date, over \$70 million has been invested in SmartKem.

Facilities in UK and Asia



What is needed

Process
temperature



Smartkem is offering a **Low-temperature** semiconductor platform

Solution-coated (**Printable**)
frontplanes, OLED and EQD



A manufacturing process
compatible with amorphous
silicon infrastructure with
higher performance



Low temperature
processing that enables
backplanes that are
solution-coated on low-
cost substrates

MicroLED Backplane requirement: Low IR drop

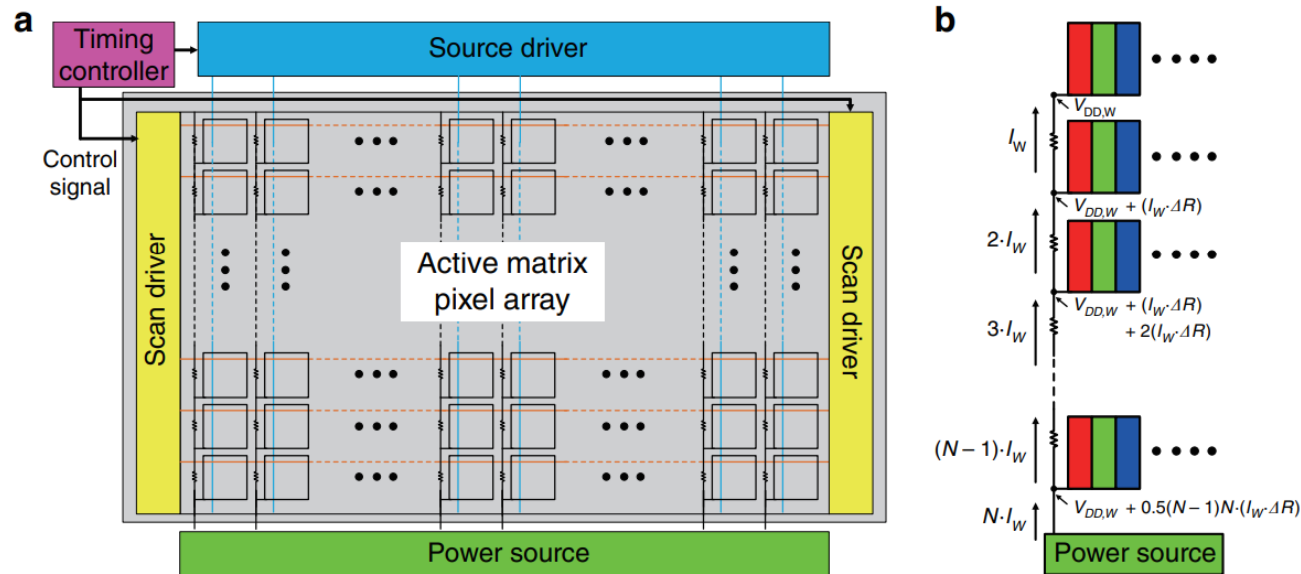


Fig. 4 Illustration of V_{DD} voltage drop. **a** System schematic of an AM panel. **b** Voltage drop on a V_{DD} line

Huang et al. Light: Science & Applications (2020)
9:105

In addressing panel performance while minimizing heating issues, adjusting the driving scheme through duty adjustment is a visible approach.

- Reducing IR drop necessitates increasing metal thickness, leading to the implementation of panel-level **RDL** (Redistribution Layer) processes.
- RDL processes require a thicker dielectric thickness ($>10\mu\text{m}$) compared to the conventional $1\mu\text{m}$ or $2\mu\text{m}$ dielectric (PFA) used in TFT-LCD

Physical properties for Conventional Dielectric vs. Warpage

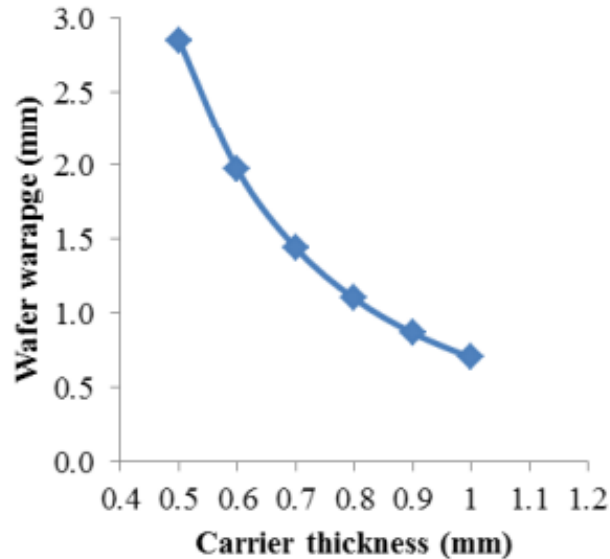
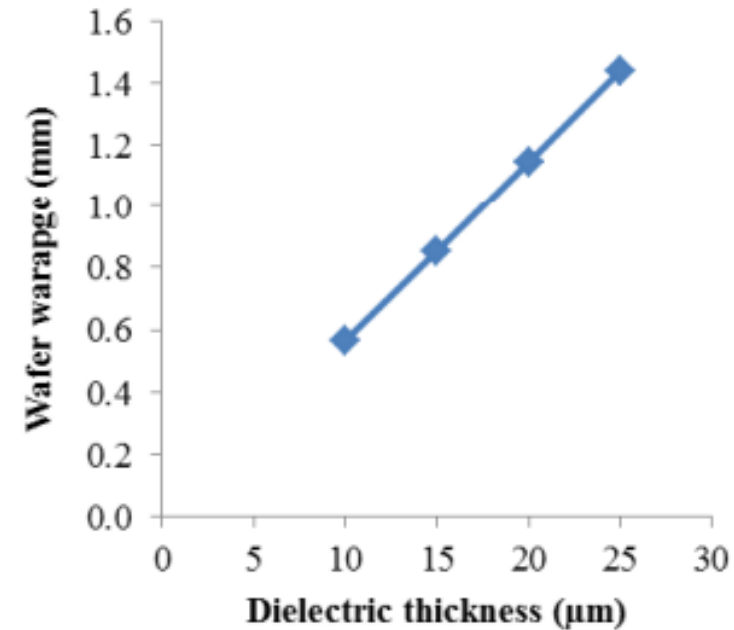


Fig. 11. Effect of glass carrier thickness on wafer warpage.

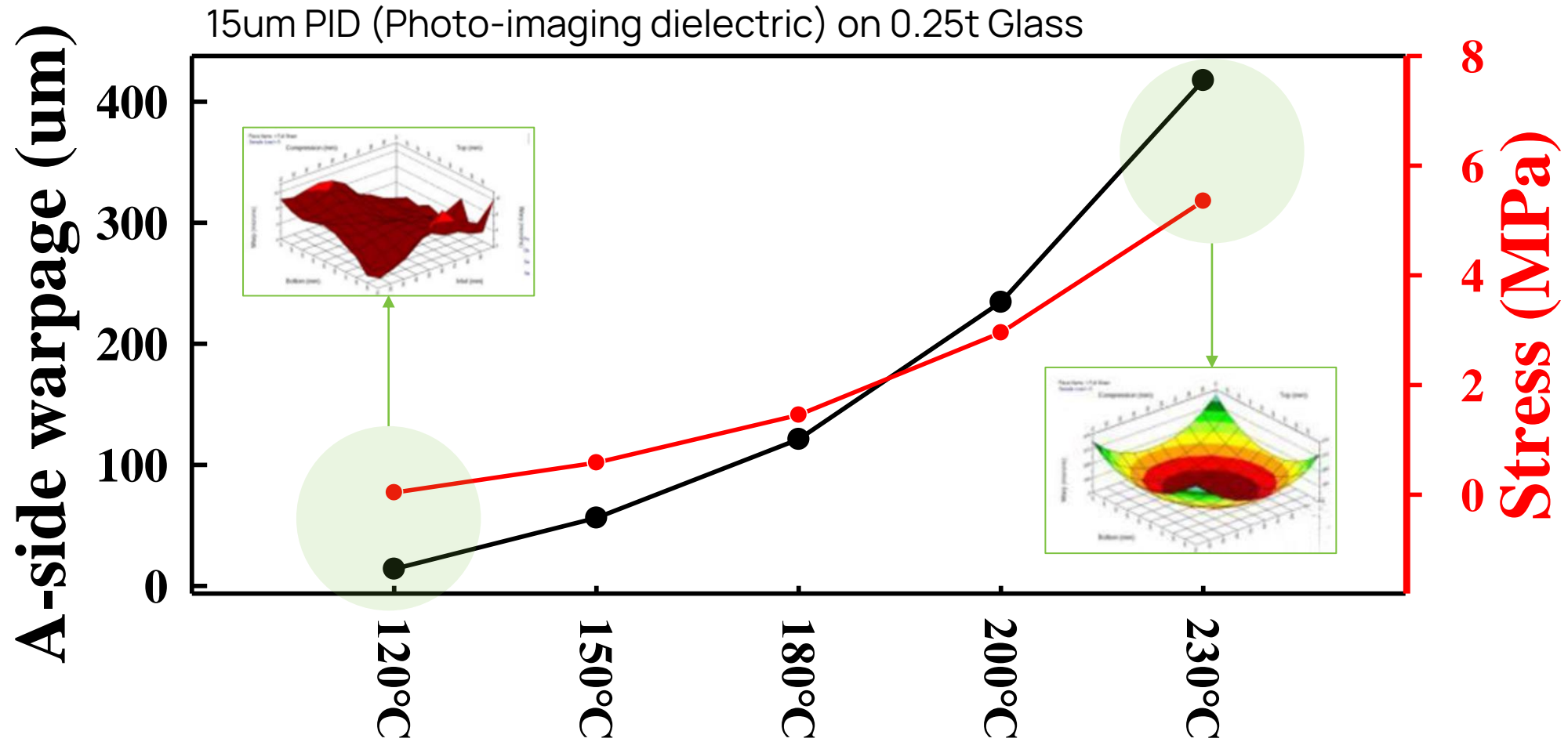


Article in IEEE Transactions on Components, Packaging, and Manufacturing Technology · December 2018
DOI: 10.1109/TCPMT.2018.2889308

Effect of PID (photo-dielectric material) on glass warpage :

When PID thickness ↑ or carrier thickness ↓ >> Warpage ↑

Temperature effect on Warpage

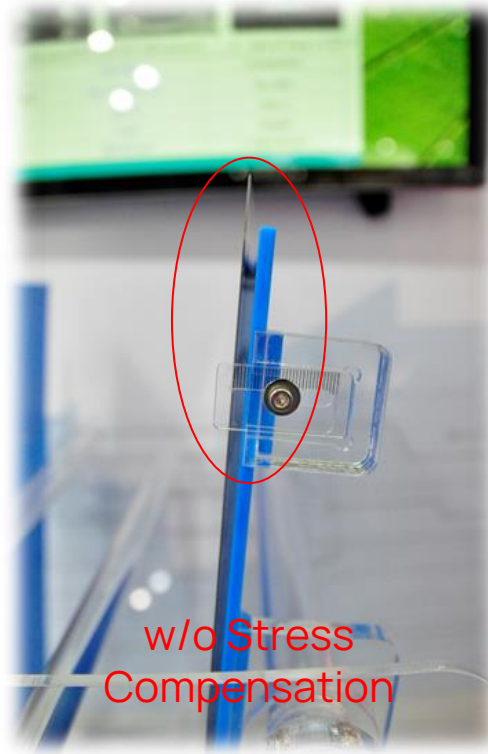


Low Warpage Solution via Low Cure (Low-Temperature)

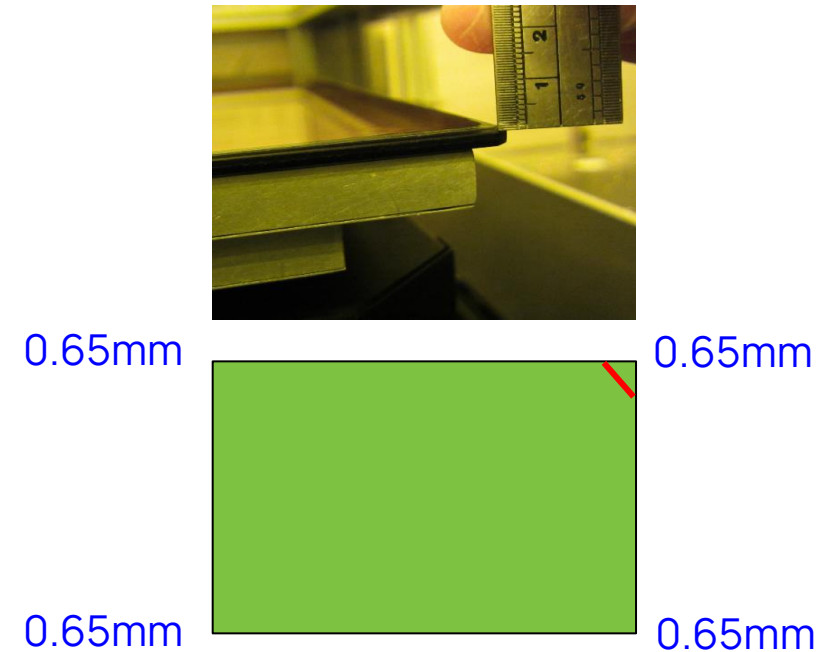
TRUFLEX® Product SPEC: Cu sheet resistance ≤ 0.002 (Ω/\square) Substrate dimension : 370mm x 470mm



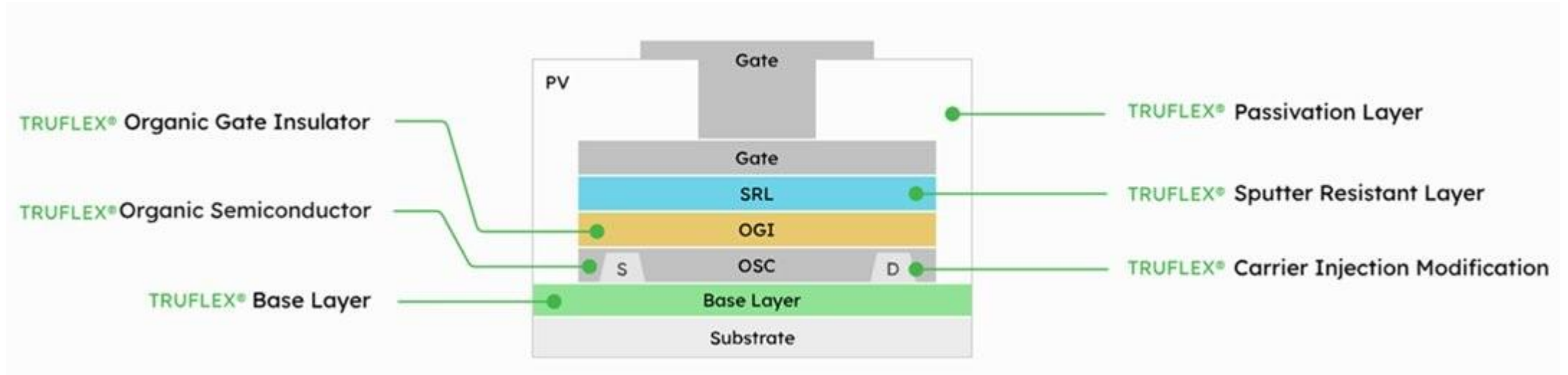
Low Warpage



High Warpage



Smartkem's TRUFLEX® Materials



Ease of
Technology Transfer

Chemistry, process and stack owned

**World leading
electronic performance**

Solution processed
At 80°C

Formed on low-cost glass & plastic

**Meets industry critical
test standards**

Drop in technology
for **today's fab lines**

(and ready for next gen printing)

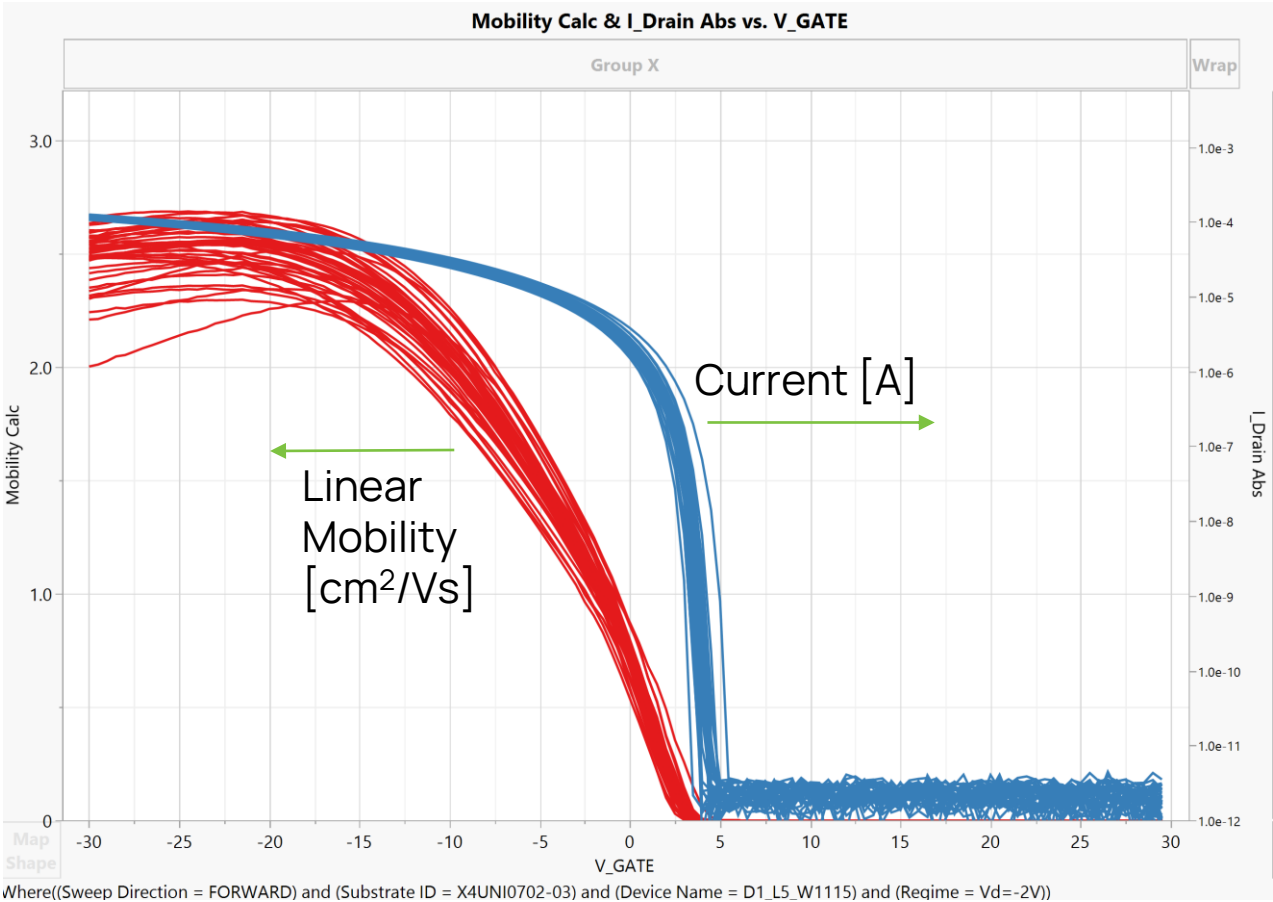
Outperforms market leader a-Si

Mobility and current uniformity – overlaid on same graph

Mobility uniformity¹ = 4.1%
Max/Min² U%=8%

$$\mu = \frac{\partial I_{DS}}{\partial V_G} \frac{L}{WC_i V_{DS}}$$

- (1) - one standard deviation
- (2) - ((max-min)/(max+min))*100

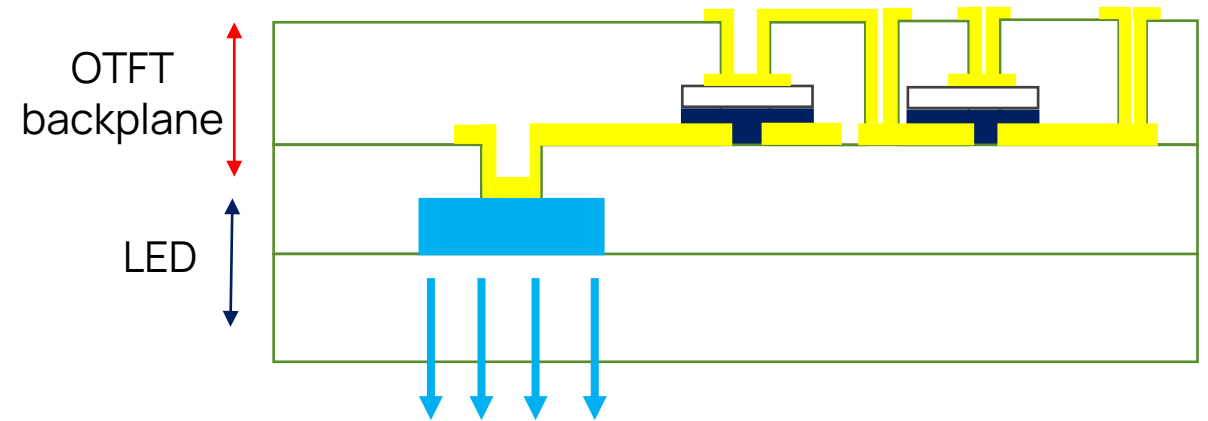


Variability Summary for Mobility											
	Mean	Std Dev	CV	Lower 95%	Upper 95%	Minimum	Maximum	Range	Median	Observations	
Mobility	2.5	0.1	4.1	2.5	2.6	2.3	2.7	0.4	2.5	41	

Variability Summary for Vto Forward											
	Mean	Std Dev	CV	Lower 95%	Upper 95%	Minimum	Maximum	Range	Median	Observations	
Vto Forward	4.6	0.4	8.5	4.5	4.7	4.0	5.5	1.5	4.5	41	

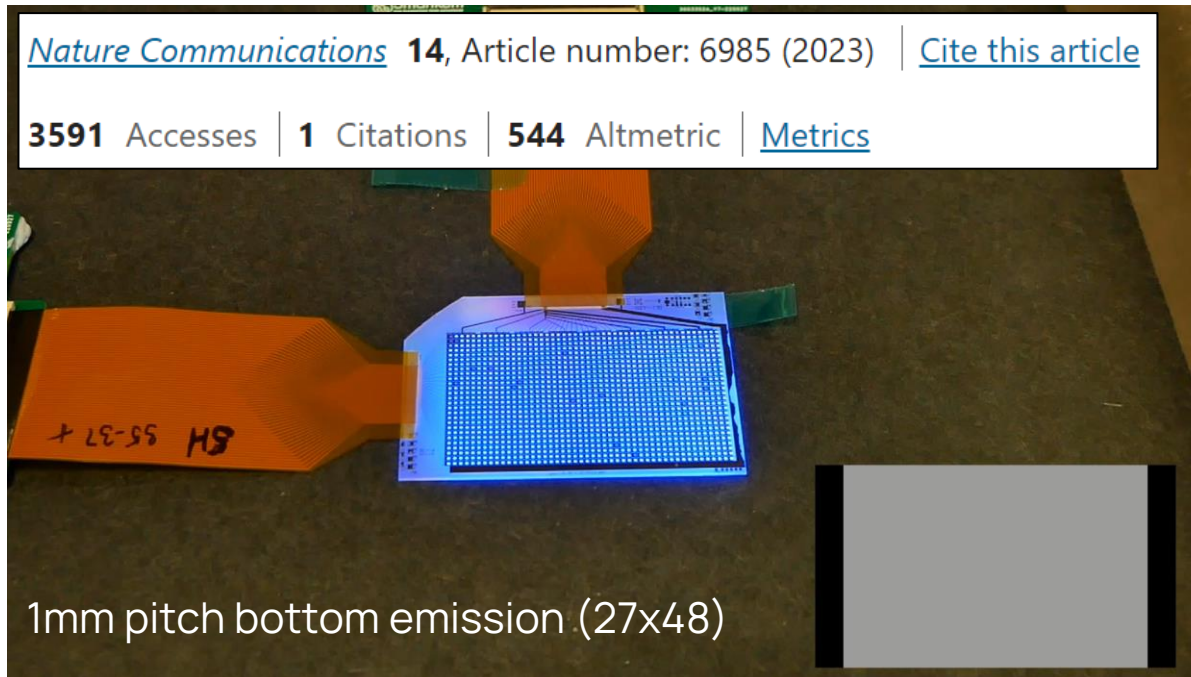
Monolithic MicroLED Via OTFTs

- Process can be scaled from **10ppi to >1000ppi** with appropriate lithography tools

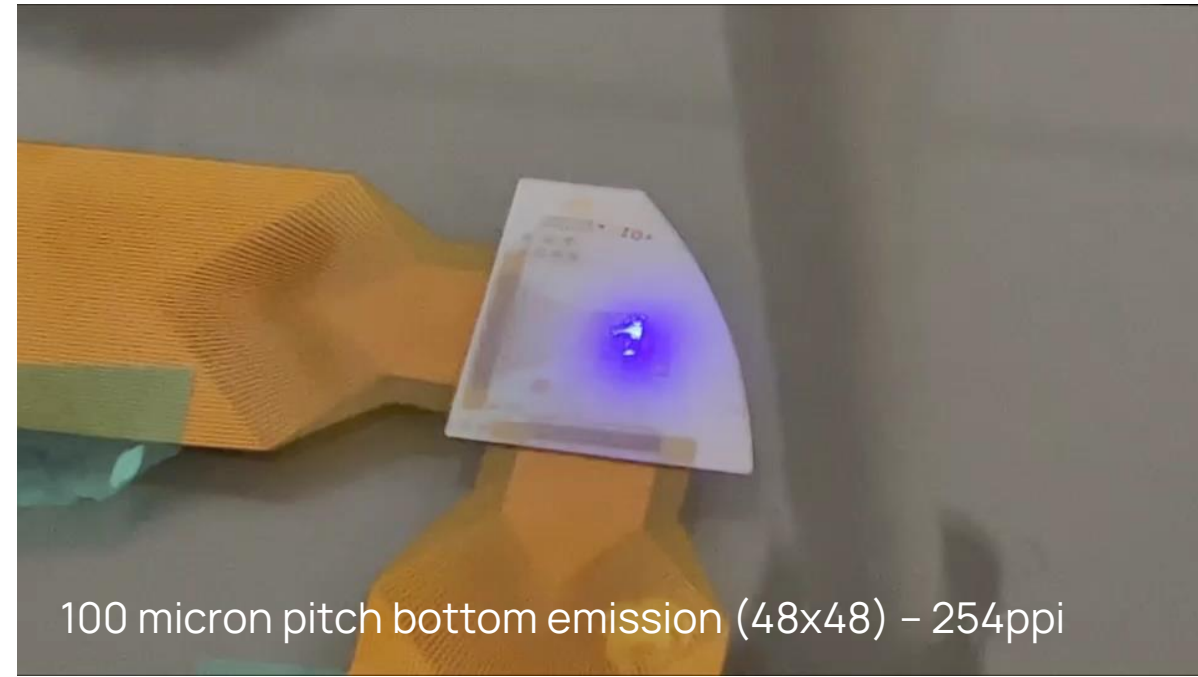


[Nature Communications](#) **14**, Article number: 6985 (2023) | [Cite this article](#)

3591 Accesses | **1** Citations | **544** Altmetric | [Metrics](#)



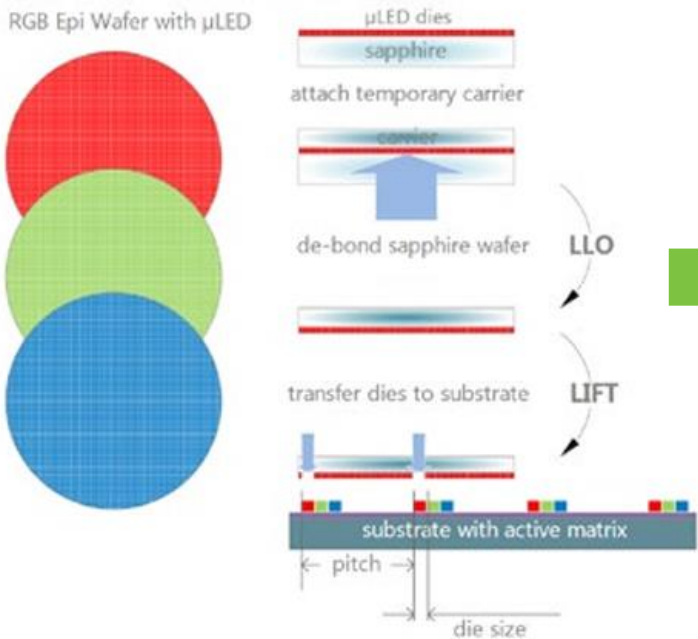
1mm pitch bottom emission (27x48)



100 micron pitch bottom emission (48x48) – 254ppi

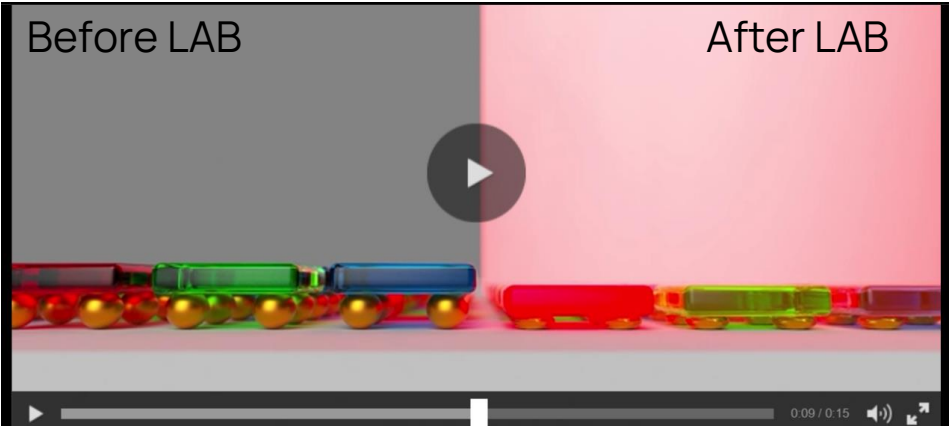
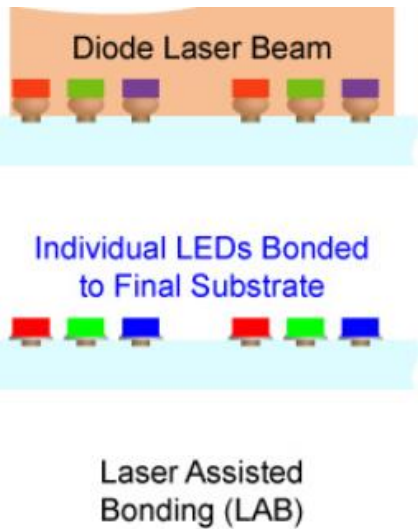
Mass Transfer Process for MicroLED Displays

LIFT (Laser induced forward transfer)



The MicroLED Association - White Papers

LAB (Laser Assisted Bonding / so called mass welding 巨量焊接)



Reference from COHERENT

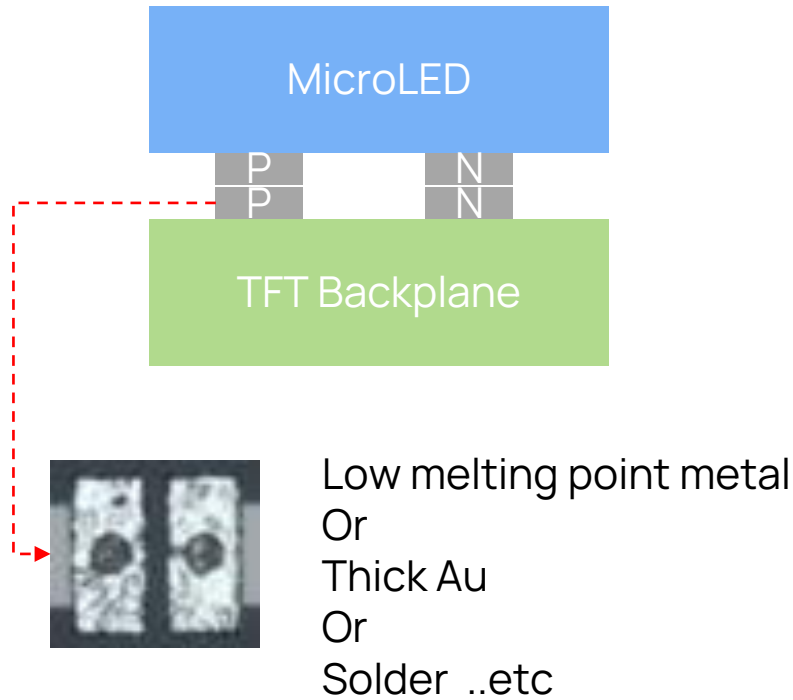
Major Yield Loss steps , Required mass repair !

Sk

MicroLED via Chip First RDL Process

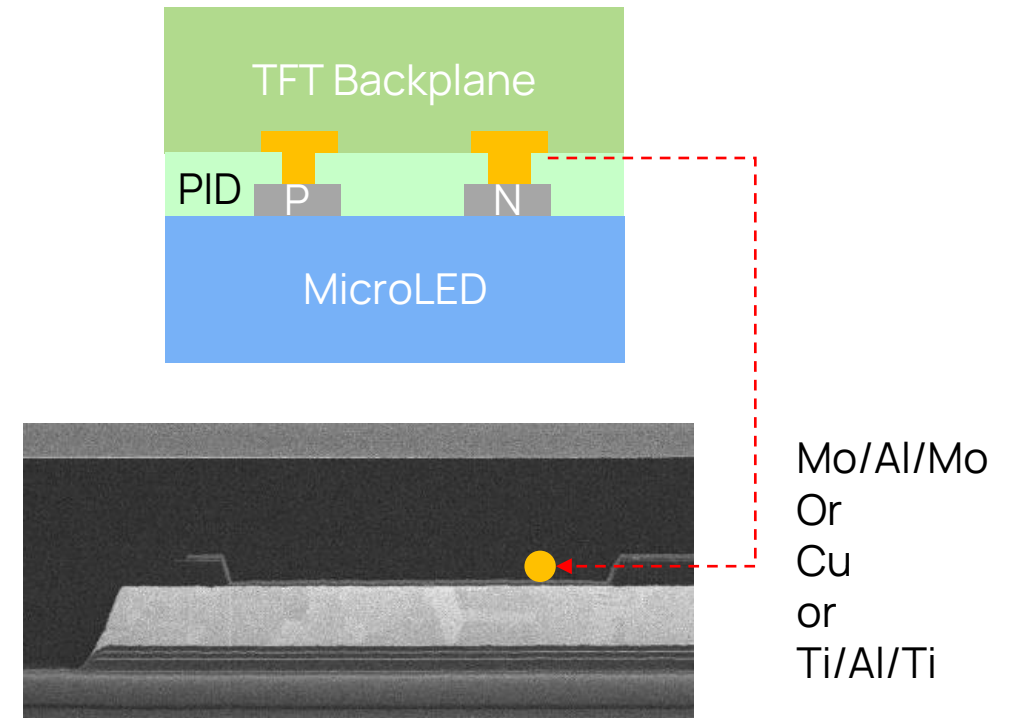
Conventional

LAB (Laser Assisted Bonding / 巨量焊接)

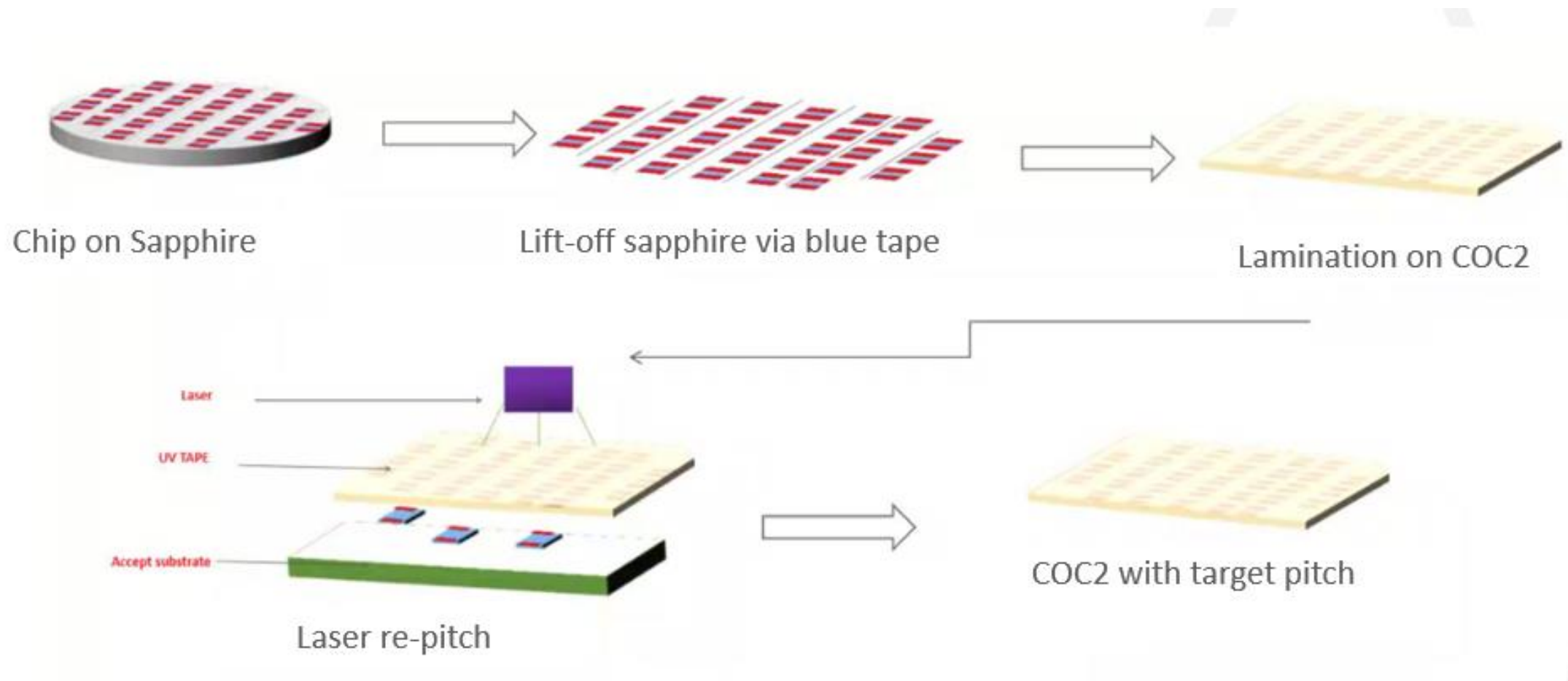


Smartkem approach

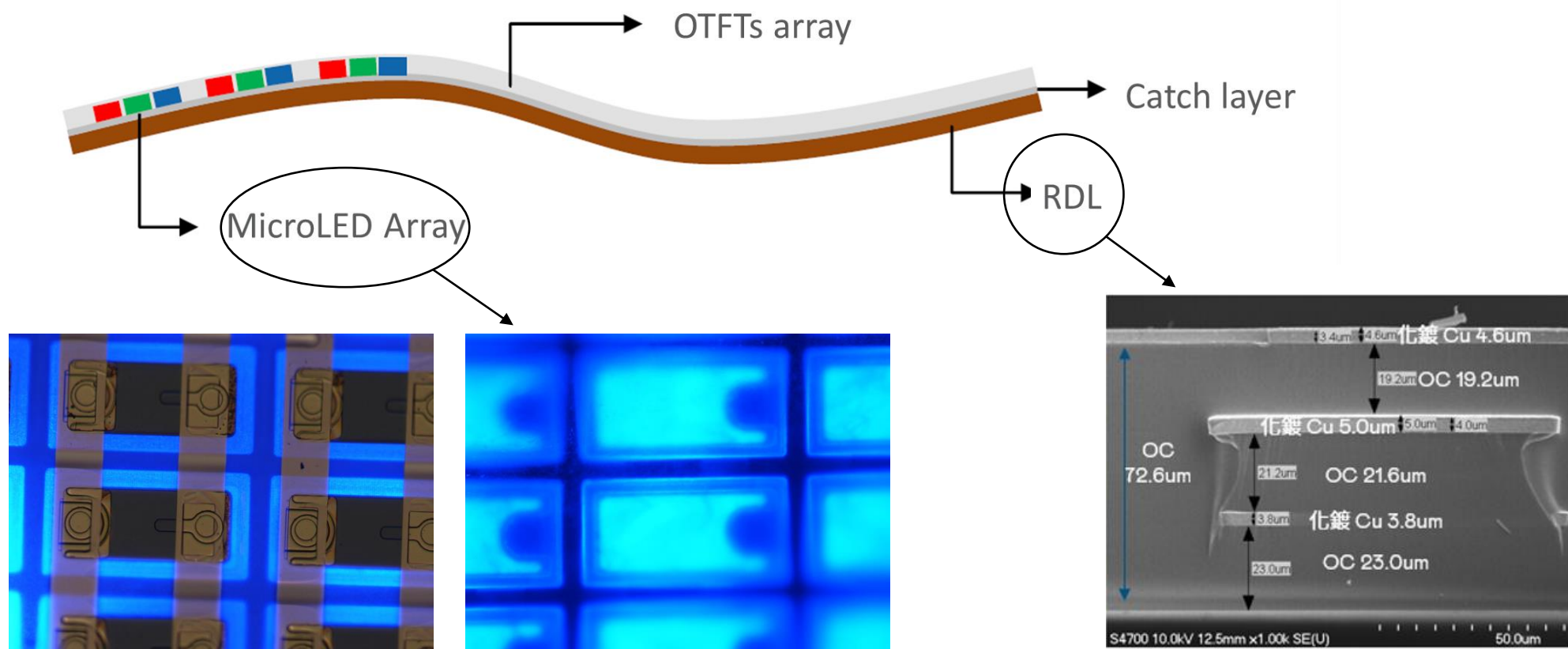
RDL Process Via PID materials



Overall MicroLED via RDL Process



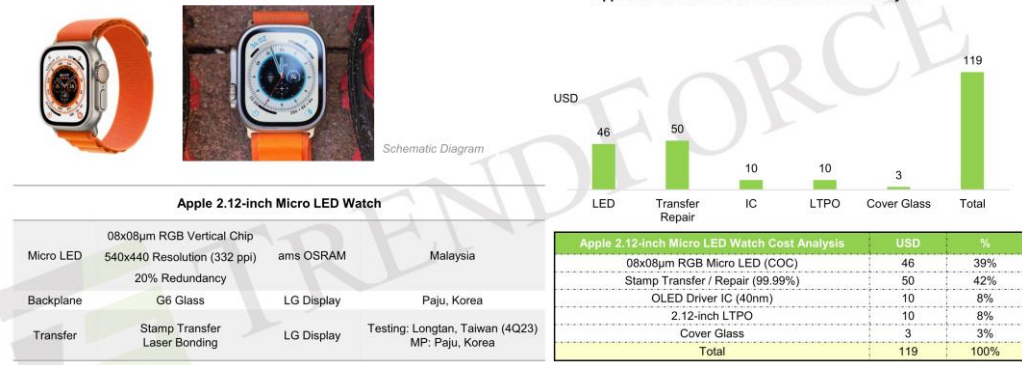
Smartkem MicroLED Displays



Our Offerings

Termination of Micro LED Apple Watch !!

TRENDFORCE



Apple 2.12-inch Micro LED Watch Cost Analysis	USD	%
08x08µm RGB Micro LED (COC)	46	39%
Stamp Transfer / Repair (99.99%)	50	42%
OLED Driver IC (40nm)	10	8%
2.12-inch LTPO	10	8%
Cover Glass	3	3%
Total	119	100%

Via Smartkem Chip-first approach

- Cost of micro-LEDs will be about \$10 for an 8x15 die size (maybe \$7 for 8x8 dies) – based on \$1000 cost of source wafer
- Remainder of COC cost will be the cost of die sorting, testing, pitch adjustment (\$39) – assume same as for 8x8um Apple case
- Stamp transfer/Repair cost could be substantially reduced if the chip-first approach is used (no transfer and 1st time yield increase of 99.99% → 99.999%) - <\$5 repair cost
- OTFT backplane cost will be < 50% of LTPO cost
- Total cost would therefore be \$72 (vs \$119) - **%40 reduction**
- Potential further reductions would come from greater efficiency in die sorting, testing and pitch adjustment (maybe blue + QD-CC approach would be lower cost)

An Introduction to the Monolithic OTFT-on-uLED Process

Exploiting SmartKem's Ultra-Low Process Temperature
to unlock novel methods of micro-LED backplane manufacturing

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Thank you

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