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Marvell Expands Custom Compute Platform with UALink Scale-up Solution for AI Accelerated Infrastructure

- *Optimized custom offering enables end-to-end UALink architecture for rack-scale AI*
- *Delivering high compute performance with low power and latency*
- *Open standards-based technology supports flexible interconnect solutions that allow customers to innovate at scale*

SANTA CLARA, Calif., June 11, 2025 /PRNewswire/ -- [Marvell Technology, Inc.](#) (NASDAQ: MRVL), a leader in data infrastructure semiconductor solutions, today announced its custom Ultra Accelerator Link (UALink) scale-up offering. As part of the Marvell® comprehensive IP portfolio for custom AI compute platforms, the new custom UALink solution delivers open standards-based scale-up interconnect with high compute utilization with low latency—enabling greater efficiency and scalability between AI accelerators and switches in next-generation accelerated infrastructure.

The Marvell custom UALink scale-up solution features a comprehensive set of interoperable IPs, including:

- Best in class 224G SerDes and UALink Physical Layer IP
- Configurable UALink Controller IP
- Scalable low-latency Switch Core and Fabric IP
- Advanced packaging options including co-packaged copper and co-packaged optics

The custom UALink solution enables customers to deliver scale-up interconnects for hundreds or thousands of AI accelerators in a scale-up deployment. Paired with Marvell custom silicon capabilities, compute vendors can build solutions including custom accelerators with UALink controllers and custom switches. The combination of Marvell advanced packaging technology and the custom UALink architecture enables optimal performance for rack-scale AI.

Hyperscalers are increasingly challenged by the need to scale AI infrastructure while ensuring high performance. The Marvell custom UALink offering addresses these challenges with an open-standards based toolkit that enables direct, low-latency communication between accelerators and supports flexible, scalable switch topologies. Marvell empowers hyperscalers to build next-generation AI infrastructure with the performance, interoperability and efficiency required to support AI workloads.

"We are pleased to introduce our new custom UALink offering to enable the next generation of AI scale-up systems," said Nick Kucharewski, senior vice president and general manager, Cloud Platform Business Unit at Marvell. "This addition to our custom portfolio enables customers with flexibility to optimize their AI infrastructure with standards-based scale-up switch and interconnect technology."

"We are excited to see UALink custom solutions from Marvell, which are essential to the future of AI," said Forrest Norrod, executive vice president and general manager, Data Center Solutions Group, AMD. "At our core, we're committed to building large-scale AI and high-performance computing solutions grounded in open standards, efficiency and strong ecosystem support. We look forward to continued collaboration within the open UALink ecosystem to advance scale-up networks."

UALink Consortium

Marvell is a member of the UALink Consortium, an open industry standard group dedicated to developing UALink specifications. The consortium drives the adoption of a connection between accelerators and related devices, enabling seamless interoperability, communication, and high-performance computing – setting new standards for AI, empowering the development of next-generation applications, and driving transformative breakthroughs in the AI era.

About Marvell

To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for over 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

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