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Intel Launches Integrated Photonics Research Center

Collaborative, multiple university center brings together world-renowned photonics and circuits researchers to pave the way for the next decade of compute interconnect.

SANTA CLARA, Calif.--(BUSINESS WIRE)-- **What's New:** Intel Labs recently opened the Intel® Research Center for Integrated Photonics for Data Center Interconnects. The center's mission is to accelerate optical input/output (I/O) technology innovation in performance scaling and integration with a specific focus on photonics technology and devices, CMOS circuits and link architecture, and package integration and fiber coupling.

> *"At Intel Labs, we're strong believers that no one organization can successfully turn all the requisite innovations into research reality. By collaborating with some of the top scientific minds from across the United States, Intel is opening the doors for the advancement of integrated photonics for the next generation of compute interconnect. We look forward to working closely with these researchers to explore how we can overcome impending performance barriers."*
> –James Jaussi, senior principal engineer and director of the PHY Research Lab in Intel Labs

Why It's Important: The ever-increasing movement of data from server to server is taxing the capabilities of today's network infrastructure. The industry is quickly approaching the practical limits of electrical I/O performance. As demand continues to increase, electrical I/O power-performance scaling is not keeping pace and will soon limit available power for compute operations. This performance barrier can be overcome by integrating compute silicon and optical I/O, a key research center focus.

Intel has recently demonstrated progress in critical technology building blocks for integrated photonics. Light generation, amplification, detection, modulation, CMOS interface circuits and package integration are essential to achieve the required performance to replace electrical as the primary high-bandwidth off-package interface.

Additionally, optical I/O has the potential to dramatically outperform electrical in the key performance metrics of reach, bandwidth density, power consumption and latency. Further innovations are necessary on several fronts to extend optical performance while lowering power and cost.

About the Research Center: The Intel Research Center for Integrated Photonics for Data Center Interconnects brings together universities and world-renowned researchers to accelerate optical I/O technology innovation in performance scaling and integration. The research vision is to explore a technology scaling path that satisfies energy efficiency and bandwidth performance requirements for the next decade and beyond.

Intel understands that academia is at the heart of technological innovation and seeks to catalyze innovation in research at leading academic institutions worldwide. Today's announcement reflects Intel's ongoing commitment to collaborate with academia in developing new and advanced technologies that improve and further computing as we know it.

The researchers participating in the Research Center include:

- **John Bowers**, University of California, Santa Barbara
  Project: Heterogeneously Integrated Quantum Dot Lasers on Silicon.
  Description: The UCSB team will investigate issues with integrating indium arsenide (InAs) quantum dot lasers with conventional silicon photonics. The goal of this project is to characterize expected performance and design parameters of single frequency and multiwavelength sources.

- **Pavan Kumar Hanumolu**, University of Illinois, Urbana-Champaign
  Project: Low-power optical transceivers enabled by duo-binary signaling and baud-rate clock recovery.
  Description: This project will develop ultra-low-power, high-sensitivity optical receivers using novel trans-impedance amplifiers and baud-rate clock and data recovery architectures. The prototype optical transceivers will be implemented in a 22 nm CMOS process to demonstrate very high jitter tolerance and excellent energy efficiency.

- **Arka Majumdar**, University of Washington
  Project: Nonvolatile reconfigurable optical switching network for high-bandwidth data communication.
  Description: The UW team will work on low-loss, nonvolatile electrically reconfigurable silicon photonic switches using emerging chalcogenide phase change materials. Unlike existing tunable mechanisms, the developed switch will hold its state, allowing zero static power consumption.

- **Samuel Palermo**, Texas A&M University
  Project: Sub-150fJ/b optical transceivers for data center interconnects.
  Description: This project will develop energy-efficient optical transceiver circuits for a massively parallel, high-density and high-capacity photonic interconnect system. The goal is to improve energy efficiency by employing dynamic voltage frequency scaling in the transceivers, low-swing voltage-mode drivers, ultra-sensitive optical receivers with tight photodetector integration, and low-power optical device tuning loops.

- **Alan Wang**, Oregon State University
  Project: 0.5V silicon microring modulators driven by high-mobility transparent conductive oxide.
  Description: This project seeks to develop a low driving voltage, high bandwidth silicon microring resonator modulator (MRM) through heterogeneous integration between the silicon MOS capacitor with high-mobility Ti:In_2O_3 The device promises to

overcome the energy efficiency bottleneck of the optical transmitter and can be co-packaged in future optical I/O systems.

- **Ming Wu**, University of California, Berkeley
  Project: Wafer-scale optical packaging of silicon photonics.
  Description: The UC Berkeley team will develop integrated waveguide lenses that have potential to enable non-contact optical packaging of fiber arrays with low loss and high tolerances.

- **S.J. Ben Yoo**, University of California, Davis
  Project: Athermal and power-efficient scalable high-capacity silicon-photonic transceivers.
  Description: The UC Davis team will develop extremely power-efficient athermal silicon-photonic modulator and resonant photodetector photonic integrated circuits scaling to 40 Tb/s capacity at 150 fJ/b energy efficiency and 16 Tb/s/mm I/O density. To achieve this, the team will also develop a new 3D packaging technology for vertical integration of photonic and electronic integrated circuits with 10,000 pad-per-square-mm interconnect-pad-density.

More Context: Intel Labs (Press Kit)

About Intel

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