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Intel Research Advances 'Era of Tera'

World's First Programmable Processor to Deliver Teraflops Performance with Remarkable Energy Efficiency

SANTA CLARA, Calif.--(BUSINESS WIRE)--

Intel Corporation researchers have developed the world's first programmable processor that delivers supercomputer-like performance from a single, 80-core chip not much larger than the size of a finger nail while using less electricity than most of today's home appliances. This is the result of the company's innovative "Tera-scale computing" research aimed at delivering Teraflops -- or trillions of calculations per second --performance for future PCs and servers. Technical details of the Teraflops research chip will be presented at the annual Integrated Solid State Circuits Conference (ISSCC) this week in San Francisco.

Tera-scale performance, and the ability to move terabytes of data, will play a pivotal role in future computers with ubiquitous access to the Internet by powering new applications for education and collaboration, as well as enabling the rise of high-definition entertainment on PCs, servers and handheld devices. For example, artificial intelligence, instant video communications, photo-realistic games, multimedia data mining and real-time speech recognition - once deemed as science fiction in "Star Trek" shows - could become everyday realities.

Intel has no plans to bring this exact chip designed with floating point cores to market. However, the company's Tera-scale research is instrumental in investigating new innovations in individual or specialized processor or core functions, the types of chip-to-chip and chip-to-computer interconnects required to best move data and, most importantly, how software will need to be designed to best leverage multiple processor cores. This Teraflops research chip offered specific insights in new silicon design methodologies, high-bandwidth interconnects and energy management approaches.

"Our researchers have achieved a wonderful and key milestone in terms of being able to drive multi-core and parallel computing performance forward," said Justin Rattner, Intel Senior Fellow and chief technology officer. "It points the way to the near future when Teraflops-capable designs will be commonplace and reshape what we can all expect from our computers and the Internet at home and in the office."

The first time Teraflops performance was achieved was in 1996, on the ASCI Red Supercomputer built by Intel for the Sandia National Laboratory. That computer took up more than 2,000 square feet, was powered by nearly 10,000 Pentium(R) Pro processors, and consumed over 500 kilowatts of electricity. Intel's research chip achieves this same performance on a multi-core chip.

Also remarkable is that this 80-core research chip achieves a teraflops of performance while

consuming only 62 watts - less than many single-core processors today.

The chip features an innovative tile design in which smaller cores are replicated as "tiles," making it easier to design a chip with many cores. With Intel's discovery of new and robust materials to build future transistors and no immediate end in sight for Moore's Law, this lays a path to manufacture multi-core processors with billions of transistors more efficiently in the future.

The Teraflops chip also features a mesh-like "network-on-a-chip" architecture that allows super-high bandwidth communications between the cores and is capable of moving Terabits of data per second inside the chip. The research also investigated methods to power cores on and off independently, so only the ones needed to complete a task are used, thus providing more energy efficiency.

Further Tera-scale research will focus on the addition of 3-D stacked memory to the chip as well as developing more sophisticated research prototypes with many general-purpose Intel(R) Architecture-based cores. Today, the Intel(R) Tera-scale Computing Research Program has more than 100 projects underway that explore other architectural, software and system design challenges.

Intel is presenting eight other papers at ISSCC, including one which will cover the Intel(R) Core(TM) micro-architecture and its use in dual and quad core processors spanning laptops to desktop PCs and servers, using both 65nm and revolutionary 45nm process technologies. Other papers cover such topics as a Radio Frequency Identification (RFID) reader transceiver chip, a low-power cache for mobile applications and a reconfigurable Viterbi accelerator in addition to novel circuits for on-die supply resonance suppression, on-chip phase-noise measurement and adaptive techniques for variations and aging.

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Source: Intel Corporation