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Intel Re-architects the Fundamental Building Block for High-Performance Computing

Next-Generation Intel® Xeon Phi™ Processor with Integrated Intel® Omni Scale Fabric to Deliver Up to 3 Times the Performance of Previous Generation at Lower Power

NEWS HIGHLIGHTS

- Announces new microarchitecture and memory details of the next-generation Intel® Xeon Phi™ processor (code-named Knights Landing), scheduled to power HPC systems in the second half of 2015.
- Intel® Omni Scale Fabric– an end-to-end interconnect optimized for fast data transfers, reduced latencies and higher efficiency – initially available as discreet components in 2015, will also be integrated into next-generation Intel Xeon Phi processor (Knights Landing) and future 14nm Intel® Xeon® processors.
- Intel continues to lead in HPC segment with 85 percent of all supercomputers on the latest TOP500* list powered by Intel Xeon processors.

LEIPZIG, Germany--(BUSINESS WIRE)-- INTERNATIONAL SUPERCOMPUTING CONFERENCE (ISC) – Intel Corporation today announced new details for its next-generation Intel® Xeon Phi™ processors, code-named Knights Landing, which promise to extend the benefits of code modernization investments being made for current generation products. These include a new high-speed fabric that will be integrated on-package and high-bandwidth, on-package memory that combined, promise to accelerate the rate of scientific discovery. Currently memory and fabrics are available as discrete components in servers limiting the performance and density of supercomputers.

The new interconnect technology, called Intel® Omni Scale Fabric, is designed to address the requirements of the next generations of high-performance computing (HPC). Intel Omni Scale Fabric will be integrated in the next generation of Intel Xeon Phi processors as well as future general-purpose Intel® Xeon® processors. This integration along with the fabric's HPC-optimized architecture is designed to address the performance, scalability, reliability, power and density requirements of future HPC deployments. It is designed to balance price and performance for entry-level through extreme-scale deployments.

"Intel is re-architecting the fundamental building block of HPC systems by integrating the Intel Omni Scale Fabric into Knights Landing, marking a significant inflection and milestone for the HPC industry," said Charles Wuischpard, vice president and general manager of Workstations and HPC at Intel. "Knights Landing will be the first true many-core processor to address today's memory and I/O performance challenges. It will allow programmers to leverage existing code and standard programming models to achieve significant

performance gains on a wide set of applications. Its platform design, programming model and balanced performance makes it the first viable step towards exascale."

Knights Landing – Unmatched Integration

Knights Landing will be available as a standalone processor mounted directly on the motherboard socket in addition to the PCIe-based card option. The socketed option removes programming complexities and bandwidth bottlenecks of data transfer over PCIe, common in GPU and accelerator solutions. Knights Landing will include up to 16GB high-bandwidth, on-package memory at launch – designed in partnership with Micron* – to deliver five times better bandwidth compared to DDR4 memory[1], five times better energy efficiency[2] and three times more density[2] than current GDDR-based memory. When combined with integrated Intel Omni Scale Fabric, the new memory solution will allow Knights Landing to be installed as an independent compute building block, saving space and energy by reducing the number of components.

Powered by more than 60 HPC-enhanced Silvermont architecture-based cores, Knights Landing is expected to deliver more than 3 TFLOPS of double-precision performance[3] and three times the single-threaded performance[4] compared with the current generation. As a standalone server processor, Knights Landing will support DDR4 system memory comparable in capacity and bandwidth to Intel Xeon processor-based platforms, enabling applications that have a much larger memory footprint. Knights Landing will be binary-compatible with Intel Xeon processors[5], making it easy for software developers to reuse the wealth of existing code.

For customers preferring discrete components and a fast upgrade path without needing to upgrade other system components, both Knights Landing and Intel Omni Scale Fabric controllers will be available as separate PCIe-based add-on cards. There is application compatibility between currently available Intel® True Scale Fabric and future Intel Omni Scale Fabric, so customers can transition to new fabric technology without change to their applications. For customers purchasing Intel True Scale Fabric today, Intel will offer a program to upgrade to Intel Omni Scale Fabric when it's available.

Knights Landing processors are scheduled to power HPC systems in the second half of 2015. For instance, in April the National Energy Research Scientific Computing Center (NERSC) announced an HPC installation planned for 2016, serving more than 5,000 users and over 700 extreme-scale science projects.

"We are excited about our partnership with Cray and Intel to develop NERSC's next supercomputer 'Cori,'" said Dr. Sudip Dosanjh, NERSC Director, Lawrence Berkeley National Laboratory. "Cori will consist of over 9,300 Intel Knights Landing processors and will serve as an on-ramp to exascale for our users through an accessible programming model. Our codes, which are often memory-bandwidth limited, will also greatly benefit from Knights Landing's high speed on package memory. We look forward to enabling new science that cannot be done on today's supercomputers."

New Fabric, New Speeds with Intel Omni Scale Fabric

Intel Omni Scale fabric is built upon a combination of enhanced acquired IP from Cray and

QLogic, and Intel's own in-house innovations. It will include a full product line offering consisting of adapters, edge switches, director switch systems, and open-source fabric management and software tools. Additionally, traditional electrical transceivers in the director switches in today's fabrics will be replaced by Intel® Silicon Photonics-based solutions, enabling increased port density, simplified cabling and reduced costs[6]. Intel Silicon Photonics-based cabling and transceiver solutions may also be used with Intel Omni Scale-based processors, adapter cards and edge switches.

Intel Supercomputing Momentum Continues

The current generation of Intel Xeon processors and Intel Xeon Phi coprocessors powers the top-rated system in the world – the 35 PFLOPS "Milky Way 2" in China. Intel Xeon Phi coprocessors are also available in more than 200 OEM designs worldwide.

Intel-based systems account for 85 percent of all supercomputers on the 43rd edition of the TOP500 list announced today and 97 percent of all new additions. Within 18 months after the introduction of Intel's first many-core architecture products, Intel Xeon Phi coprocessor-based systems already make up 18 percent of the aggregated performance of all TOP500 supercomputers. The complete TOP500 list is available at www.top500.org.

To help optimize applications for many-core processing, Intel has also established more than 30 Intel Parallel Computing Centers (IPCC) in cooperation with universities and research facilities around the world. Today's parallel optimization investment with the Intel Xeon Phi coprocessor will carry forward to Knights Landing, as optimizations using standards-based, common programming languages persist with a recompile. Incremental tuning gains will be available to take advantage of innovative new functionality.

About Intel

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1 Projected result based on internal Intel analysis of STREAM benchmark using a Knights Landing processor with 16GB of high-bandwidth versus DDR4 memory only with all channels populated

2 Projected results based on internal Intel analysis of Knights Landing's on-package memory MCDRAM vs Knights Corner's GDDR5 memory

3 Internal and preliminary projections of theoretical double-precision performance measured by Linpack. Based on current expectations of Knights Landing's cores, clock frequency and floating point operations per cycle.

4. Projected peak theoretical single-thread performance relative to 1st Generation Intel® Xeon Phi™ Coprocessor 7120P (formerly code-named Knights Corner)

5 Binary Compatible with Intel Xeon processors using Haswell Instruction Set (except TSX - Transactional Synchronization Extensions)

6 The TCO or other cost reduction scenarios described in this document are intended to enable you to get a better understanding of how the purchase of a given Intel product, combined with a number of situation-specific variables, might affect your future cost and savings. Circumstances will vary and there may be unaccounted-for costs related to the use and deployment of a given product. Nothing in this document should be interpreted as either a promise of or contract for a given level of costs."

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