



## Intel Reveals Details of Next-Generation High-Performance Computing Platforms

**Intel® Xeon® E5 Processor Debuts on TOP500 List; First Intel® Many Integrated Core Co-processor Demonstrated to Deliver Performance Above 1 TFLOPS**

### NEWS HIGHLIGHTS

- Intel® Xeon® processor E5 family, world's first server chip to support the PCI Express\* 3.0 I/O integration, debuts on TOP500 list, powering 10 supercomputers.
- Intel's "Knights Corner" product, the first commercial co-processor based on the Intel® Many Integrated Core (Intel® MIC) architecture, was shown for the first time breaking the barrier of 1 TFLOPS double precision performance\*\*.
- Intel announced additional investments and new partner projects with R&D laboratories to pursue the goal of achieving Exascale performance by 2018.
- Intel processors power 85 percent of all new entries to the latest TOP500 list of supercomputers, with Intel Xeon processor 5600 series being most popular selected for 223 systems.

SEATTLE--(BUSINESS WIRE)-- At [SC11](#), Intel Corporation revealed details about the company's next-generation Intel Xeon processor-based and [Intel® Many Integrated Core \(Intel® MIC\)](#)-based platforms designed for high-performance computing (HPC). The company also outlined new investments in research and development that will lead the industry to Exascale performance by 2018.

During his briefing at the conference, Rajeeb Hazra, general manager of Technical Computing, Intel Datacenter and Connected Systems Group, said that the Intel Xeon processor E5 family is the world's first server processor to support full integration of the PCI Express 3.0 specification\*\*. PCIe 3.0 is estimated\*\* to double the interconnect bandwidth over the PCIe\* 2.0 specification\*\* while enabling lower power and higher density server implementations. New fabric controllers taking advantage of the PCI Express 3.0 specification will allow more efficient scaling of performance and data transfer with the growing number of nodes in HPC supercomputers.

The early-performance benchmarks revealed that the Intel Xeon E5 delivers up to 2.1\* times\*\* more performance in raw FLOPS (Floating Point Operations Per Second as measured by Linpack\*) and up to 70 percent more performance using real-HPC workloads compared to the previous generation of Intel Xeon 5600 series processors.

"Customer acceptance of the Intel Xeon E5 processor has exceeded our expectations and is driving the fastest debut on the TOP500 list of any processor in Intel's history," said Hazra. "Collecting, analyzing and sharing large amounts of information is critical to today's science activities and requires new levels of processor performance and technologies designed precisely for this purpose."

The Intel Xeon E5 processors made their way onto the TOP500 list in the year of the 40<sup>th</sup> anniversary of availability of the world's first microprocessor (the Intel 4004 processor) and on the 10<sup>th</sup> anniversary of the launch of the Intel Xeon brand. Since the introduction of Intel Xeon processors in 2001, Intel estimates that Xeon processor performance has increased by more than 130 times\*\*\*.

Two months since its initial shipments to supercomputer centers, Intel Xeon E5 processors now power 10 systems on the [TOP500](#) list. More than 20,000 of these processors are in operation, delivering a cumulative peak performance of more than 3.4 Petaflops.

As previously announced, the upcoming Intel Xeon processor E5 family will power several other future supercomputers, including the 10 PFLOPS ["Stampede"](#) at Texas Advanced Computing Center, the 1.6 PFLOPS ["Yellowstone"](#) at The National Center for Atmospheric Research, the 1.6 PFLOPS ["Curie"](#) at GENCI, the 1.3 PFLOPS system at International Fusion Energy Research Center ([IFERC](#)) and more than 1 PFLOPS ["Pleiades"](#) expansion at NASA.

Intel started shipping the Intel Xeon processor E5 family to a small number of cloud and HPC customers in September, with broad availability planned in the first half of 2012. Intel is tracking more than 400 design wins for the Intel Xeon processor E5 family, nearly double the amount at time of launch of the Xeon 5500/5600 generation. Demand for initial production units is approximately 20 times greater than for previous generations of the Intel Xeon 5500 or 5600 series processors.

During SC'11 Intel also provided details on its greatly expanded lineup of server boards and chassis, including products specifically optimized for HPC, which will be ready to support the launch of the Intel® Xeon® Processor E5.

### **First Teraflops Intel Many Integrated Core Co-Processor Showcased**

Intel also reiterated its commitment to delivering the most efficient and programming-friendly platform for highly parallel applications. The benefits of the Intel MIC architecture in weather modelling, tomography, proteins folding and advanced materials simulation were shown at Intel's booth at SC'11.

The first presentation of the first silicon of "Knights Corner" co-processor showed that Intel architecture is capable of delivering more than 1 TFLOPs of double precision floating point performance (as measured by the Double-precision, General Matrix-Matrix multiplication benchmark -- DGEMM\*). This was the first demonstration of a single processing chip capable of achieving such a performance level.

"Intel first demonstrated a Teraflop supercomputer utilizing 9,680 Intel® Pentium Pro® Processors in 1997 as part of Sandia Lab's "ASCI RED" system," Hazra said. "Having this performance now in a single chip based on Intel MIC architecture is a milestone that will once again be etched into HPC history."

"Knights Corner," the first commercial Intel MIC architecture product, will be manufactured using Intel's latest 3-D Tri-Gate 22nm transistor process and will feature more than 50 cores. When available, Intel MIC products will offer both high performance from an architecture specifically designed to process highly parallel workloads, and compatibility with existing x86 programming model and tools.

Hazra said that the "Knights Corner" co-processor is very unique as, unlike traditional accelerators, it is fully accessible and programmable like fully functional HPC compute node, visible to applications as though it was a computer that runs its own Linux\*-based operating system independent of the host OS.

One of the benefits of Intel MIC architecture is the ability to run existing applications without the need to port the code to a new programming environment. This will allow scientists to use both CPU and co-processor performance simultaneously with existing x86 based applications, dramatically saving time, cost and resources that would otherwise be needed to rewrite them to alternative proprietary languages.

### **Intel Increases Investment in Exascale Computing Labs**

As previously [announced](#) at the International Supercomputing Conference 2011 in Hamburg, Germany, Intel's goal is to deliver Exascale-level performance by 2018 (which is more than 100 times faster performance than is currently available) while only requiring two times the power usage of the current top supercomputer. Fundamental to achieving that goal is working closely with the HPC community, and today Hazra announced several new initiatives that will help to achieve that goal.

Intel and the Barcelona Supercomputing Center (BSC) have signed a multi-year agreement to create the Exascale Laboratory in Barcelona, Intel's fourth European Exascale R&D lab that joins existing sites in Paris, Juelich (Germany) and Lueven (Belgium). This new laboratory will focus on scalability issues in the programming and runtime systems of Exascale supercomputers.

Additionally, the Science and Technology Facilities Council (STFC) and Intel have signed a memorandum of understanding to develop and test technology that will be required to power the supercomputers of tomorrow. Under this initial agreement, STFC's computational scientists at its Daresbury Laboratory in England and Intel will work together to test and evaluate Intel's current and future hardware with leading software applications to ensure that scientists are ready to exploit Intel's supercomputer systems of the future.

### **TOP500 Supercomputers**

The 38<sup>th</sup> edition of the Top500 list, which was announced at SC'11, shows that the world's leading scientists and institutions continue to base their supercomputers on Intel Xeon processors. Out of all new entries to the list compared to last edition, Intel-powered supercomputers accounted for close to 85 percent. The [Intel Xeon 5600 series](#) processor is the top processor on the list, powering 223 systems. Intel Xeon processor E5 family made its introduction in 10 systems on the list with record-breaking 152 GFLOPS per socket and 91 percent efficiency. Intel processors also power five systems in the top 10 and almost 77 percent of all listed supercomputers. The complete report is available at [www.top500.org](http://www.top500.org).

More information on SC'11, including Hazra's presentation and pictures, are available at [www.intel.com/newsroom/sc11](http://www.intel.com/newsroom/sc11).

## About Intel

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\* Other brands and names may be claimed as the property of others.

\*\* Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark\* and MobileMark\*, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

Configurations [Intel Xeon E5 vs Intel Xeon 5600 performance claims]:

- 2S Xeon E5 score of 342.7 based on Intel internal measurements as of 7 September 2011 using an Intel Rose City platform with two Intel® Xeon® processor E5, Turbo Enabled, EIST Enabled, Hyper-Threading Enabled, 64 GB memory (8 x 8GB DDR3-1600), Red Hat\* Enterprise Linux Server 6.1 beta for x86\_64
- Intel Tylersburg-EP platform with two Intel® Xeon® Processor X5690 (6-Core, 3.46GHz, 12MB L3 cache, 6.4GT/s, B1-stepping), EIST Enabled, Turbo Boost enabled, Hyper-Threading Disabled, 48GB memory (12x 4GB DDR3-1333 REG ECC), 160GB SATA 7200RPM HDD, Red Hat\* Enterprise Linux Server 5.5 for x86\_64 with kernel 2.6.35.10. Source: Intel internal testing as of Apr 2011. Score : 159.40 Gflops.

Intel internal measurements October 2011. For more information go to [www.intel.com/performance](http://www.intel.com/performance).

\*\*\* Results have been estimated based on internal Intel analysis and are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance.

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