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# Intel Equipped to Lead Industry to Era of Exascale Computing

Intel(R) Many Integrated Core (Intel(R) MIC) Architecture Shows Strength as Critical Component of Intel's Exascale Computing Solution

## NEWS HIGHLIGHTS

- With collaboration partners, Intel aims to deliver complete technology solution for exascale performance by the end of the decade.
- Demonstrations from key supercomputing centers such as Forschungszentrum Juelich, Leibniz Supercomputing Centre, CERN and KISTI underscore momentum of Intel(R) Many Integrated Core Architecture.
- Intel processor-powered supercomputers make up 77 percent of the latest TOP500 list of supercomputers and nearly 90 percent of all new systems in 2011.

SANTA CLARA, Calif. & HAMBURG, Germany--(BUSINESS WIRE)-- At the International Supercomputing Conference (ISC), Kirk Skaugen, Intel Corporation vice president and general manager of the Data Center Group, outlined the company's vision to achieve ExaFLOP/s performance by the end of this decade. An ExaFLOP/s is quintillion computer operations per second, hundreds times more than today's fastest supercomputers.

Reaching exascale levels of performance in the future will not only require the combined efforts of industry and governments, but also approaches being pioneered by the [Intel\(R\) Many Integrated Core \(Intel\(R\) MIC\) Architecture](#), according to Skaugen. Managing the explosive growth in the amount of data shared across the Internet, finding solutions to climate change, managing the growing costs of accessing resources such as oil and gas, and a multitude of other challenges require increased amounts of computing resources that only increasingly high-performing supercomputers can address.

"While [Intel\(R\) Xeon\(R\) processors](#) are the clear architecture of choice for the current TOP500 list of supercomputers, Intel is further expanding its focus on high-performance computing by enabling the industry for the next frontier with our Many Integrated Core architecture for petascale and future exascale workloads," said Skaugen. "Intel is uniquely equipped with unparalleled manufacturing technologies, new architecture innovations and a familiar software programming environment that will bring us closer to this exciting exascale goal."

## Paving the Way to Exaflop Performance

Intel's relentless pursuit of [Moore's Law](#) -- doubling the transistor density on microprocessors roughly every 2 years to increase functionality and performance while decreasing costs -- combined with an innovative, highly efficient software programming model and extreme system scalability were noted by Skaugen as key ingredients for crossing the threshold of

petascale computing into a new era of exascale computing. With this increase in performance, though, comes a significant increase in power consumption.

As an example, for today's fastest supercomputer in China, the Tianhe-1A, to achieve exascale performance, it would require more than 1.6 GW of power - an amount large enough to supply electricity to 2 million homes - thus presenting an energy efficiency challenge.

To address this challenge, Intel and European researchers have established three European labs with three main goals: to create a sustained partner presence in Europe; take advantage of the growing relevance of European high-performance computing (HPC) research; and exponentially grow capabilities in computational science, engineering and strategic computing. One of the technical goals of these labs is to create simulation applications that begin to address the energy efficiency challenges of moving to exascale performance.

Skaugen said there is the potential for tremendous growth of the HPC market. While supercomputers from the 1980s delivered GigaFLOP/s (billions of floating point operations per second) performance, today's most powerful machines have increased this value by several million times. This, in turn, has increased the demand for processors used in supercomputing. By 2013 Intel expects the top 100 supercomputers in the world to use one million processors. By 2015 this number is expected to double, and is forecasted to reach 8 million units by the end of the decade. The performance of the TOP500 #1 system is estimated to reach 100 PetaFLOP/s in 2015 and break the barrier of 1 ExaFLOP/s in 2018. By the end of the decade the fastest system on Earth is forecasted to be able to provide performance of more than 4 ExaFLOP/s.

#### Intel MIC Architecture Software Development Momentum

The Intel MIC architecture is a key addition to the company's existing products, including Intel Xeon processors, and expected to help lead the industry into the era of exascale computing. The first Intel MIC product, codenamed "Knights Corner," is planned for production on Intel's 22-nanometer technology that featuring innovative [3-D Tri-Gate transistors](#)<sup>1</sup>. Intel is currently shipping Intel MIC software development platforms, codenamed "Knights Ferry," to select development partners.

At ISC, Intel and some of its partners including Forschungszentrum Juelich, Leibniz Supercomputing Centre (LRZ), CERN and Korea Institute of Science and Technology Information (KISTI) showed early results of their work with the "Knights Ferry" platform. The demonstrations showed how Intel MIC architecture delivers both performance and software programmability advantages.

"The programming model advantage of Intel MIC architecture enabled us to quickly scale our applications running on Intel Xeon processors to the Knights Ferry Software Development Platform," said Prof. Arndt Bode of the Leibniz Supercomputing Centre. "This workload was originally developed and optimized for Intel Xeon processors but due to the familiarity of the programming model we could optimize the code for the Intel MIC architecture within hours and also achieved over 650 GFLOPS of performance."

Intel also showed server and workstation platforms from SGI, Dell, HP, IBM, Colfax and

Supermicro, all of which are working with Intel to plan products based on "Knights Corner."

"SGI recognizes the significance of inter-processor communications, power, density and usability when architecting for exascale," said SGI CTO Dr. Eng Lim Goh. "The Intel MIC products will satisfy all four of these priorities, especially with their anticipated increase in compute density coupled with familiar X86 programming environment."

## TOP500 Supercomputers

The 37<sup>th</sup> edition of the Top500 list, which was announced at ISC, shows that Intel continues to be a force in high-performance computing, with 387 systems or more than 77 percent, powered by Intel processors. Out of all new systems to the list in 2011, Intel powered systems accounted for close to 90 percent. More than half of these new additions are based on latest 32nm [Intel Xeon 5600 series](#) processors which now alone power more than 35% of all systems in TOP500 list, three times the amount comparing to last year. Intel also powers 5 systems in top 10.

The semi-annual TOP500 list of supercomputers is the work of Hans Meuer of the University of Mannheim, Erich Strohmaier and Horst Simon of the U.S. Department of Energy's National Energy Research Scientific Computing Center, and Jack Dongarra of the University of Tennessee. The complete report is available at [www.top500.org](http://www.top500.org).

More information on ISC'11 including detailed description of showcased Intel MIC architecture-based demos and performance, Skaugen's presentation and pictures are available at <http://newsroom.intel.com/docs/DOC-2152>.

## About Intel

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<sup>1</sup> [http://newsroom.intel.com/community/intel\\_newsroom/blog/2011/05/04/intel-reinvents-transistors-using-new-3-d-structure](http://newsroom.intel.com/community/intel_newsroom/blog/2011/05/04/intel-reinvents-transistors-using-new-3-d-structure) Copyright (C) 2011 Intel Corporation. All rights reserved. Intel, Xeon and the Intel logo are trademarks or registered trademarks of Intel Corporation in the U.S. and/or other countries. "MIC" is pronounced "Mike" / mahyk / m k

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