Intel Completes Next Generation, 32nm Process Development Phase

SANTA CLARA, Calif., Dec. 9, 2008 – Intel Corporation has completed the development phase of its next-generation manufacturing process that further shrinks chip circuitry to 32 nanometers (a billionth of a meter). The company is on track for production readiness of this future generation using even more energy-efficient, denser and higher performing transistors in the fourth quarter of 2009.

Intel will provide a multitude of technical details around the 32nm process technology along with several other topics during presentations at the International Electron Devices meeting (IEDM) next week in San Francisco. Finishing the development phase for the company's 32nm process technology and production readiness in this timeframe means that Intel remains on pace with its ambitious product and manufacturing cadence referred to as the company's "tick-tock" strategy.

That plan revolves around introducing an entirely new processor microarchitecture alternating with a cutting edge manufacturing process about every 12 months, an effort unmatched in the industry. Producing 32nm chips next year would mark the fourth consecutive year Intel has met its goal.

The Intel 32nm paper and presentation describe a logic technology that incorporates second-generation high-k + metal gate technology, 193nm immersion lithography for critical patterning layers and enhanced transistor strain techniques. These features enhance the performance and energy efficiency of Intel processors. Intel's manufacturing process has the highest transistor performance and the highest transistor density of any reported 32nm technology in the industry.

"Our manufacturing prowess and resulting products have helped us widen our lead in computing performance and battery life for Intel-based laptops, servers and desktops," said Mark Bohr, Intel Senior Fellow and director of process architecture and integration. "As we've shown this year, the manufacturing strategy and execution have also given us the ability to create entirely new product lines for MIDs, CE equipment, embedded computers and netbooks."

Other Intel IEDM papers will describe a low power system on chip version of Intel's 45nm process, transistors based on compound semiconductors, substrate engineering to improve performance of 45nm transistors, integrating chemical mechanical polish for the 45nm node and beyond; and, integrating an array of silicon photonics modulators. Intel will also participate in a short course on 22nm CMOS Technology.