FINANCIAL ANALYST DAY 2022

tegether we advance

Technology Leadership

Mark Papermaster
Chief Technology Officer and Executive Vice President, Technology and Engineering
CAUTIONARY STATEMENT

This presentation contains forward-looking statements concerning Advanced Micro Devices, Inc. (AMD) including, but not limited to, the timing, availability, features, functionality and expected benefits of AMD's products; AMD's R&D investment; and AMD's CPU core roadmap, which are made pursuant to the Safe Harbor provisions of the Private Securities Litigation Reform Act of 1995. Forward-looking statements are commonly identified by words such as "would," "may," "expects," "believes," "plans," "intends," "projects" and other terms with similar meaning. Investors are cautioned that the forward-looking statements in this presentation are based on current beliefs, assumptions and expectations, speak only as of the date of this presentation and involve risks and uncertainties that could cause actual results to differ materially from current expectations. Such statements are subject to certain known and unknown risks and uncertainties, many of which are difficult to predict and generally beyond AMD's control, that could cause actual results and other future events to differ materially from those expressed in, or implied or projected by, the forward-looking information and statements. Investors are urged to review in detail the risks and uncertainties in AMD’s Securities and Exchange Commission filings, including but not limited to AMD’s most recent reports on Forms 10-K and 10-Q.

AMD does not assume, and hereby disclaims, any obligation to update forward-looking statements made in this presentation, except as may be required by law.
INNOVATION KEEPS AMD ON HIGH PERFORMANCE PACE

Moore’s Law is Slowing

Chiplet Integration Enables Generational Performance Gains, Keeps AMD on Historic Pace

Heterogeneous Computing Driving Leadership Performance

Source: AMD
AMD

BROADEST HIGH PERFORMANCE IP PORTFOLIO

CPUs

GPUs

AMD XDNA and AI Engines

FPGAs and Adaptive SoCs

SmartNICs and DPUs
HIGH PERFORMANCE

CPU CORE ROADMAP

2019 — 2024

"Zen 2"

"Zen 3" 3D V-Cache

"Zen 4"

"Zen 4" 3D V-Cache

"Zen 4c"

"Zen 5" 3D V-Cache

"Zen 5c"

All roadmaps are subject to change.
LEADERSHIP HIGH PERFORMANCE EFFICIENCY

45% | Less Area vs. Competitor

45% | Lower Power vs. Competitor

78% | Better Perf/Watt vs. Competitor

<table>
<thead>
<tr>
<th></th>
<th>AMD “Zen 3” Core</th>
<th>Intel Alder Lake Golden Cove Core</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Node</strong></td>
<td>TSMC 7nm</td>
<td>Intel 7nm Process</td>
</tr>
<tr>
<td><strong>Core + L2 Area</strong></td>
<td>4.11 mm²</td>
<td>7.46 mm²</td>
</tr>
<tr>
<td><strong>8C 16T Power at 3.9G</strong></td>
<td>43.61W</td>
<td>76.7W</td>
</tr>
<tr>
<td><strong>16C 32T Perf/Watt</strong></td>
<td>1.78</td>
<td>1.0</td>
</tr>
</tbody>
</table>

See endnotes Z4-006.
WORLD’S FIRST HIGH PERFORMANCE

x86 5nm CPU

- Significant generational performance-per-watt and frequency improvement
- 8-10% instructions per clock increase
- >15% single thread performance gain
- Up to 125% memory bandwidth per core
- ISA extensions for AI and AVX-512

For servers, notebooks and desktops

Performance estimates subject to change, see endnotes Z4-001, R4-150 and Z4-002.
HIGHER PERFORMANCE WITH LOWER POWER CONSUMPTION

Performance-Per-Watt Gains

>25%

Zen 3  Zen 4

Overall Performance Improvement

>35%

Zen 3  Zen 4

“Zen” Desktop 16C 32T Performance, Cinebench NT
See endnotes Z4-003 and Z4-004.
COMING IN 2024
NEW GROUNDS-UP MICROARCHITECTURE

- Enhanced performance and efficiency
- Re-pipelined front end and wide issue
- Integrated AI and Machine Learning optimizations
LEADERSHIP HIGH-PERFORMANCE COMPUTE PLATFORM

AMD Infinity Architecture
Decade long investment in computing and modular fabric architecture

Chiplet Leadership
Heterogeneous compute engines and memory configurations in 2.5D and 3D chiplet packaging

Leadership Compute Platform
Enabled by AMD Infinity Architecture modularity and leading chiplet portfolio
SCALING HORIZONTALLY AND VERTICALLY

2.5D Elevated Fanout Bridge

- **Scalable Solution**: Lithographically Defined
- **Standard Flip Chip Process**: Lower Complexity Bumping, Assembly Process
- **Standard Substrates**: Lower Cost

3D Hybrid Bonding

- **>3X**: Interconnect Energy Efficiency Compared to Micro Bump 3D
- **>15X**: Interconnect Density Compared to Micro Bump 3D

See endnotes EPYC-26 and EPYC-27.
CHIPLET AND PACKAGING LEADERSHIP

2015: AMD 2.5D HBM
2017: Multichip Module
2019: Chiplets
2021: AMD 3D V-Cache™
2022: MI200 2.5D EFB

World’s Highest Capacity FPGA in 20nm
World’s Highest Capacity FPGA in 16nm
Versal™ Premium
Versal 2.5D

3D/2.5D HYBRID COMPUTE FUTURE

2015: XILINX
2015: XILINX
2019: XILINX
2021: XILINX
2022: XILINX
AMD INFINITY ARCHITECTURE
AMD MODULAR STRATEGY FOUNDATION

1st Gen
- CPU connectivity
- Common fabric and methodology
- Scalable data and control

2nd Gen
- 4/8-way GPU connectivity
- CPU multi-node chiplet
- Advanced chiplet design enablement

3rd Gen
- Up to 8-way GPU connectivity
- Coherent memory between EPYC™ CPUs and Instinct™ GPUs
- Exascale CPU and GPU compute

2017 2019 2021
INTRODUCING 4TH GEN AMD INFINITY ARCHITECTURE

- Enables 2.5D and 3D chiplet integration with unified system level coherency
- Extensions for Xilinx and 3rd party IP
- CXL™ 2.0-based memory for disaggregation
- Extensible architecture for CXL 3.0 and UCIe standards
CHIPLET PLATFORM LEADERSHIP

AMD is the industry leader in chiplet product deployment with >40 chiplet standard products in manufacturing

- Multi-node solutions with wide range of IP combinations
- Low latency, coherent and power efficient memory and cache
- Xilinx adaptable compute chiplets
- Custom-ready heterogeneous platform for 3rd party and customer IP chiplets
OUR PATH FORWARD

RELENTLESS INNOVATION

- Consistent delivery of leadership CPU
- Industry’s broadest high performance IP portfolio with leadership chiplet flexibility
- No let up in innovation to power the future
ENDNOTES

Z4-006: Testing by AMD Performance Labs as of May 22, 2022. Performance per watt evaluated by dividing Cinebench R23 nT score by wall power of otherwise identical systems. Alder Lake system: Core i9-12900KS, ROG Maximus Z690 Hero (BIOS 0702), 2x16GB DDR5-5200 at 392W. Zen 3 system: Ryzen 9 5950X, ROG Crosshair VIII Hero, 2x8GB DDR4-3600. All systems configured with Radeon RX 6950XT (driver 22.10 Prime), Windows 11 build 22000.593, Samsung 980 Pro 1TB SSD, Asetek 280MM liquid cooler at 203W. Results may vary based on system configuration and other variables.

Z4-001: IPC uplift based on the average of estimated/published 2017 SPECint® and 2017 SPECfp® scores and internal estimates/testing on Cinebench R23 1T and Geekbench 5 1T for “Zen4” and “Zen 3” processors.


Z4-002: Preliminary specification for 96-core Zen 4 are 12 channels of DDR5 memory compared to 64-core EPYC™ 7763 processor with 64-cores and 8 channels of DDR4 memory. Calculation is per core using 64-cores per processor.

Z4-003: Testing as of May 31, 2022, by AMD Performance Labs. Power measured at CPU socket only (Watts), CPU performance (“points”) measured with Cinebench R23 nT. AMD Ryzen 9 5950X System: AMD Reference X570 Motherboard, 2x8 DDR4-3200. AMD Ryzen 7000 Series: AMD Reference X670 Motherboard, Ryzen 7000 Series 16-core pre-production processor sample, 2x16GB DDR5-5200. All systems configured with Radeon™ RX 6950XT GPU (driver: 22.10 Prime), Windows 11 Build 22000.593, Samsung 980 Pro 1TB SSD, Asetek 280MM liquid cooler. Results may vary when final products are released in market.

Z4-004: Testing as of May 5, 2022, by AMD Performance Labs. Single-thread performance evaluated with Cinebench R23 1T. AMD Ryzen9 5950X System: ASUS ROG Crosshair VIII Hero X570, 2x8 DDR4-3600C16. AMD Ryzen 7000 Series: AMD Reference X670 Motherboard, Ryzen 7000 Series 16-core pre-production processor sample, 2x16GB DDR5-6000CL30. All systems configured with Radeon™ RX 6950XT GPU (driver: 22.10 Prime), Windows 11 Build 22000.593, Samsung 980 Pro 1TB SSD, Asetek 280MM liquid cooler. Results may vary when final products are released in market.

EPYC-026: Based on calculated areal density and based on bump pitch between AMD hybrid bond AMD 3D V-Cache stacked technology compared to AMD 2D chiplet technology and Intel 3D stacked micro-bump technology.

EPYC-027: Based on AMD internal simulations and published Intel data on “Foveros” technology specifications.