
SmartKem
Display • Performance • Chemistry

# Moore’s law and the display industry

**Ian Jenks**
*CEO*

# Forward Looking Statements

**This presentation contains forward-looking statements about SmartKem Inc. based on management's current expectations which are subject to known and unknown uncertainties and risks.**

Words such as "anticipated," "initiate," "expect," "intend," "plan," "believe," "seek," "estimate," "may," and variations of these words or similar expressions are intended to identify forward-looking statements. Our actual results could differ materially from those discussed due to a number of factors, including, but not limited to, our ability to raise additional equity and debt financing on favorable terms, the success of our products under development and other risk factors.

**We are providing this information as of the date of this presentation and do not undertake any obligation to update any forward-looking statements contained in this presentation as a result of new information, future events or otherwise. Unless the context requires otherwise, references to "SmartKem," "Company," "we," "us" and "our" refer to SmartKem Ltd.**

# Company **Overview**

## Enabling today's flexible electronics

- Founded in 2009
- Employees: 38 FTEs including 14 PhDs
- Funding to date: $60M+
- 200+ PhD years in the development of organic semiconductors
- 8,000ft$^2$ R&D facility in Manchester, UK
- Foundry service for prototyping at UK's Centre for Process Innovation (CPI)
- Extensive IP portfolio comprising 16 patent families
  (~120 issued patents; 15 pending & > 30 codified company trade secrets)

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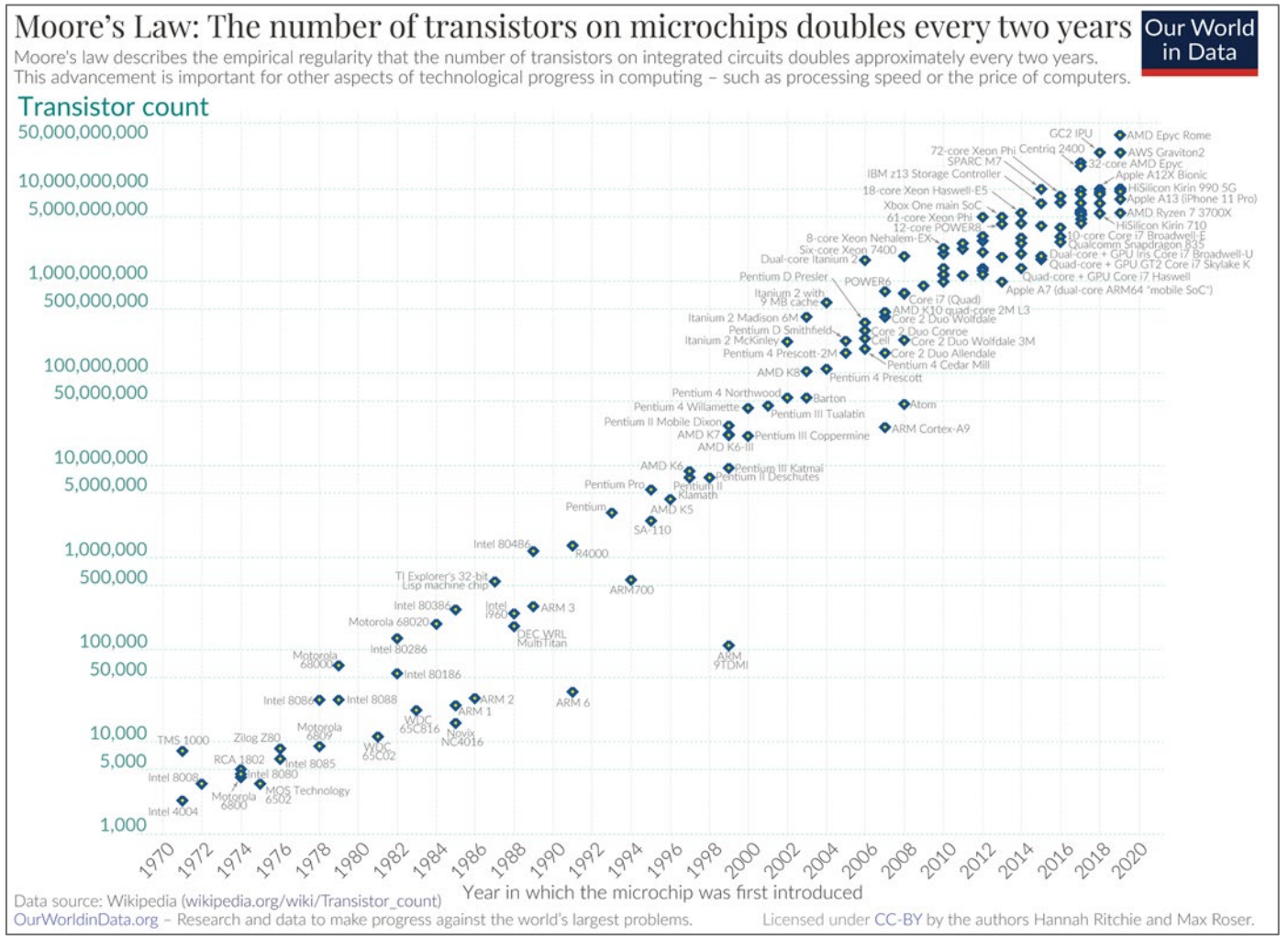
# Moore’s Law

- **Moore’s law is the observation that the number of transistor in a dense integrated circuit (IC) doubles about every two years. It is an observation and projection of an historical trend. Rather than a law of physics, it is an empirical relationship linked to gains from experience in production.**




# Sometimes I sits and think, sometimes I just sits

**If silicon transistors are free and we only need a few thousand for a display, why aren't all backplanes made of silicon?**

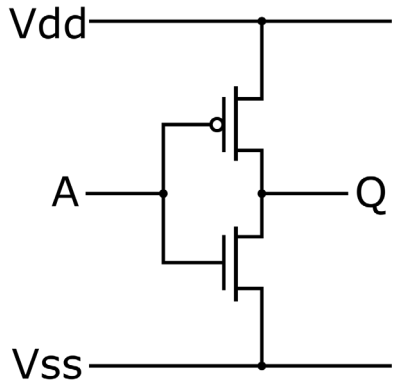
# Large area processing

| Parameter | SmartKem OTFT | a-Si | IGZO | LTPS |
|---|---|---|---|---|
| Current Usage | In development (demonstrated in e-paper, LCD and OLED) | LCD and rigid e-paper | OLED TV and some tablet LCD | Mobile phone (OLED and some LCD) |
| Typical Charge Mobility in Display Pixel | 3 $cm^2/Vs$ | 0.5 $cm^2/Vs$ | 10 $cm^2/Vs$ | 50+ $cm^2/Vs$ |
| Process Temperature | 80˚C* | 300 ˚C | 320 ˚C | 350 ˚C |
| Substrate Compatibility | Wide range of plastics and glass | Glass | PI/glass | PI/glass |
| Current Driving Stability | Very Good | Average | Very Good | Excellent |
| Off Current | Excellent | Average | Excellent | Average |
| Impact Resistance | Excellent | Poor | Poor | Poor |
| Bend Radius | 0.5mm | 4mm | 2mm | 4mm |
| Manufacturing Maturity | Prototype | Excellent | Fair | Good |
| Process Cost | Low | Low | Medium/High | Medium/High |

**If an IC only needs a small number of transistors then why aren't they made on display lines?**

# CMOS inverter logic

CMOS TFT design uses a p and n type TFT with gates connected



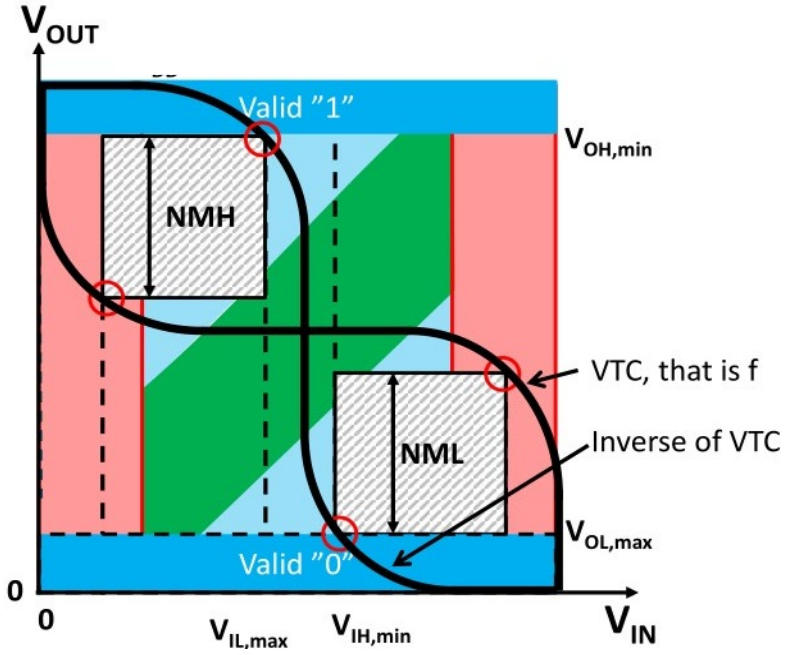

## Advantages

- Low power consumption (only have to change charge on gate of TFT) – no resistive loads consuming power
- Fast switching (if p and n devices are well matched)
- Rail to rail switching with high gain. Large noise margin

## Disadvantages

- Need a greater number photomasks and processes (to define the p-type and n-type diffused-in regions)

"Butterfly diagram" showing the wide tolerance of the CMOS inverter to variations in device Vth

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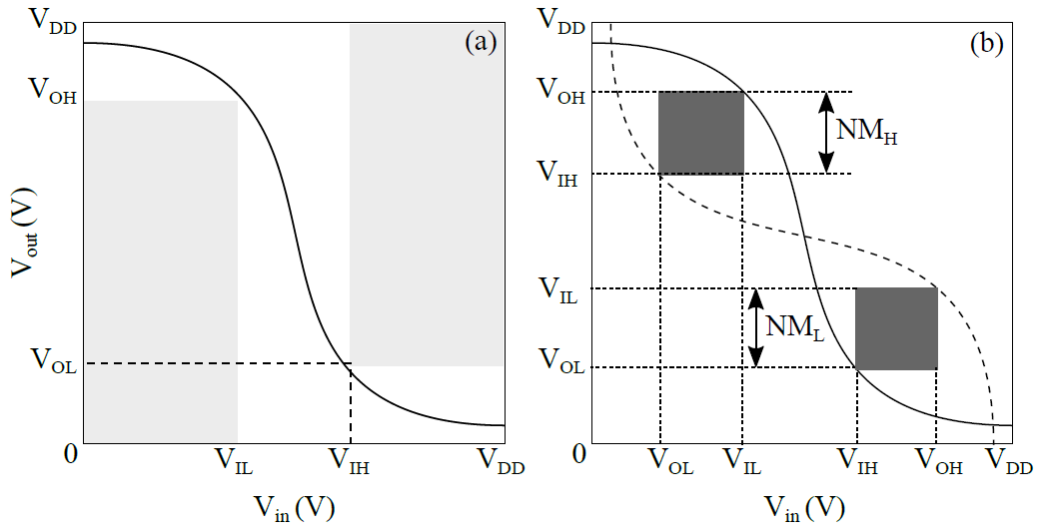
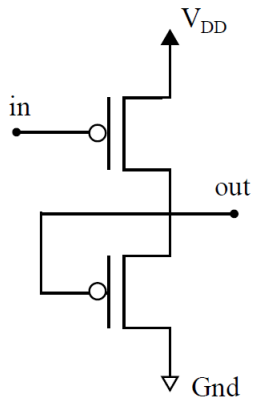
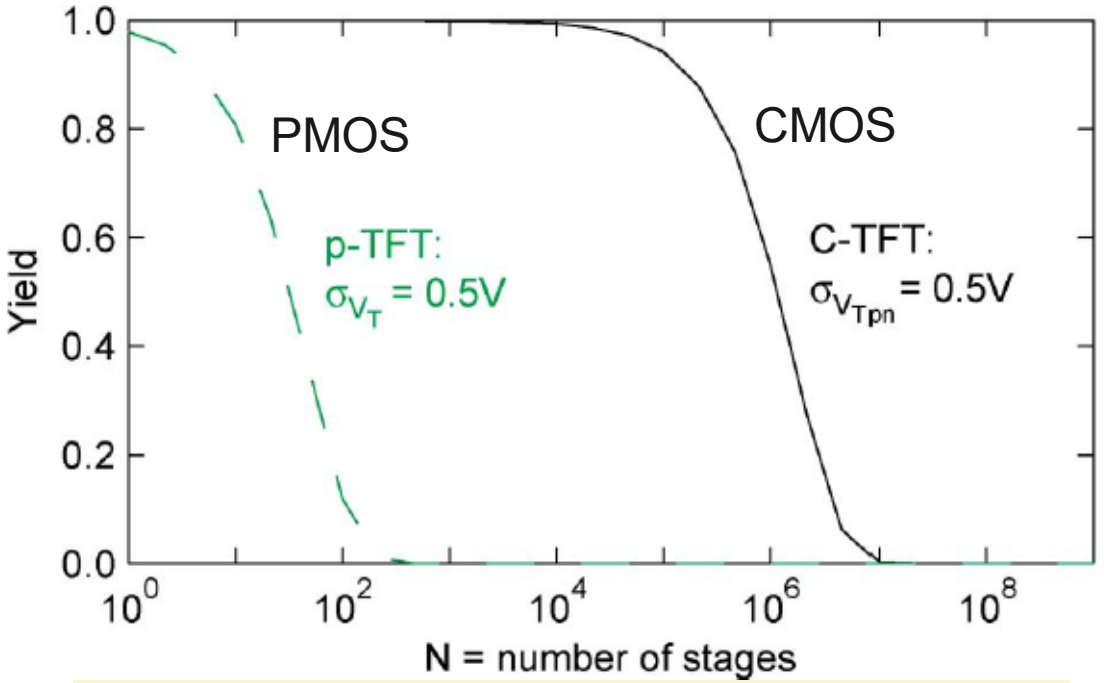
# PMOS inverters vs CMOS inverters




- PMOS inverter – a transistor load is used for pull-up and pull-down of the voltage output
- Noise margin and gain is lower than for CMOS




D. Bode *et al.*, IEEE Trans. El. Dev **57**, 201 (2010)

Comparing CMOS with PMOS for the same spread of Vth in transistors, CMOS can yield circuits of with 10,000 times more stages

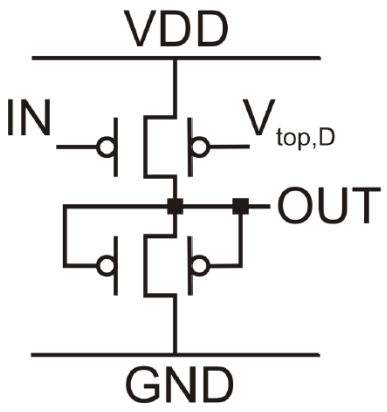
# Pseudo CMOS

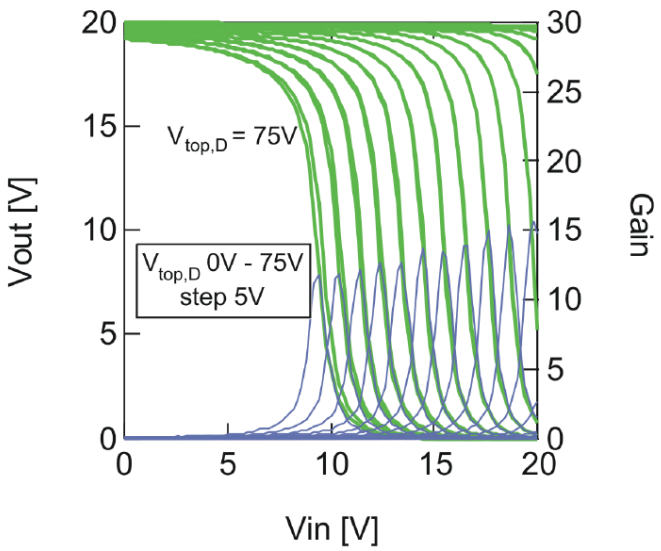
- *Pseudo CMOS* is a term for designs of logic that emulate some of the benefits of CMOS but often use NMOS or PMOS only transistors (hence avoid the processing complexity)
- Pseudo CMOS approach will follow the work of IMEC which showed that it is possible to widen the noise margin of transistors using dual gate OTFT technology to make 2 types of OTFT with different threshold voltages

2010 IEEE International Solid-State Circuits Conference

**7.4 Robust Digital Design in Organic Electronics by Dual-Gate Technology**

Kris Myny[1,2,5], Monique J. Beenhakkers[3], Nick A. J. M. van Aerle[3], Gerwin H. Gelinck[4], Jan Genoe[1,5], Wim Dehaene[1,2], Paul Heremans[1,2]



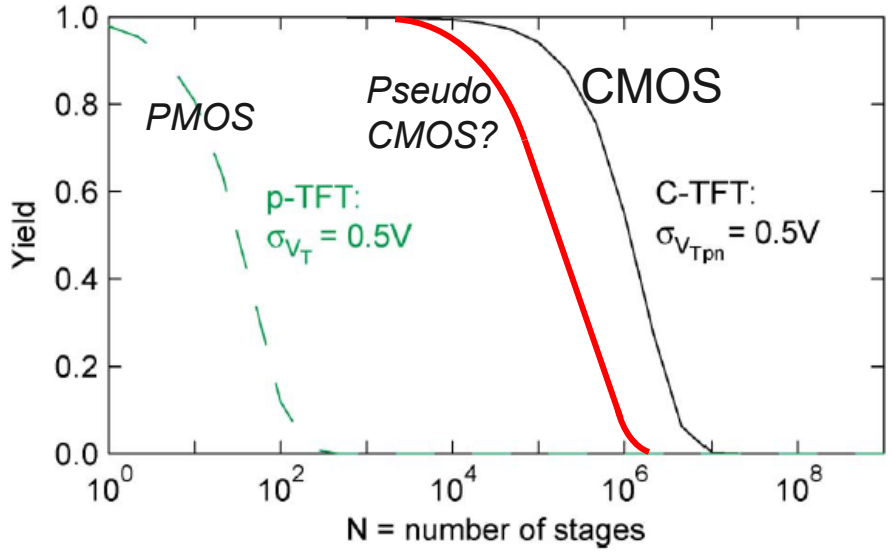

**Advantage**

- Can integrate many transistors in a circuit without failure due to Vt variations
- Only requires 1 more mask than PMOS only

**Disadvantage**

- Still uses more power than CMOS due to load TFT

Pseudo CMOS is predicted to achieve similar yield to CMOS in larger circuits

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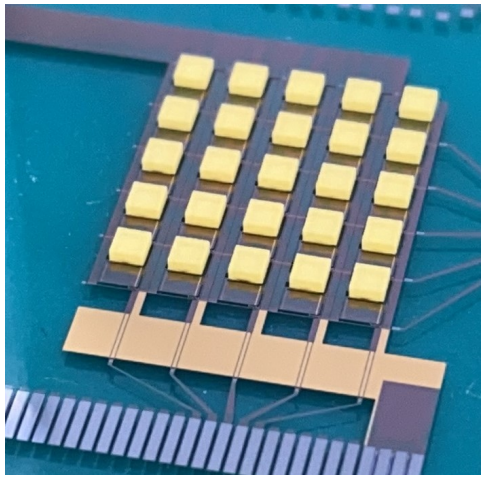
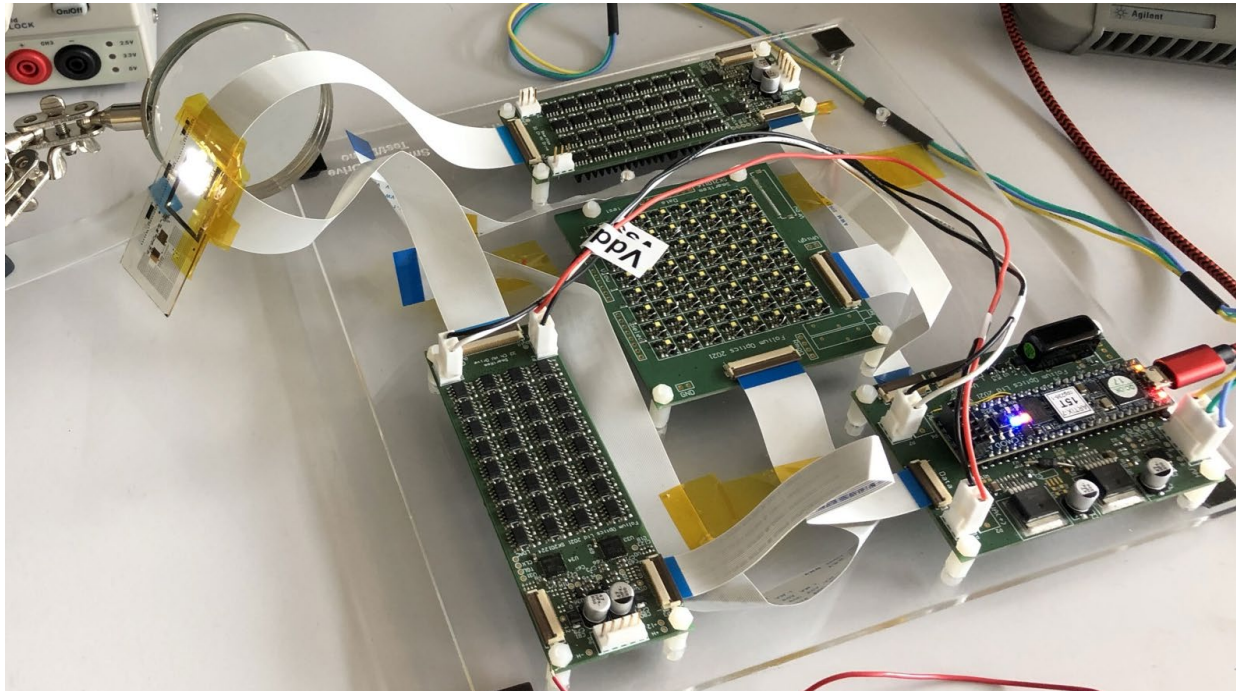
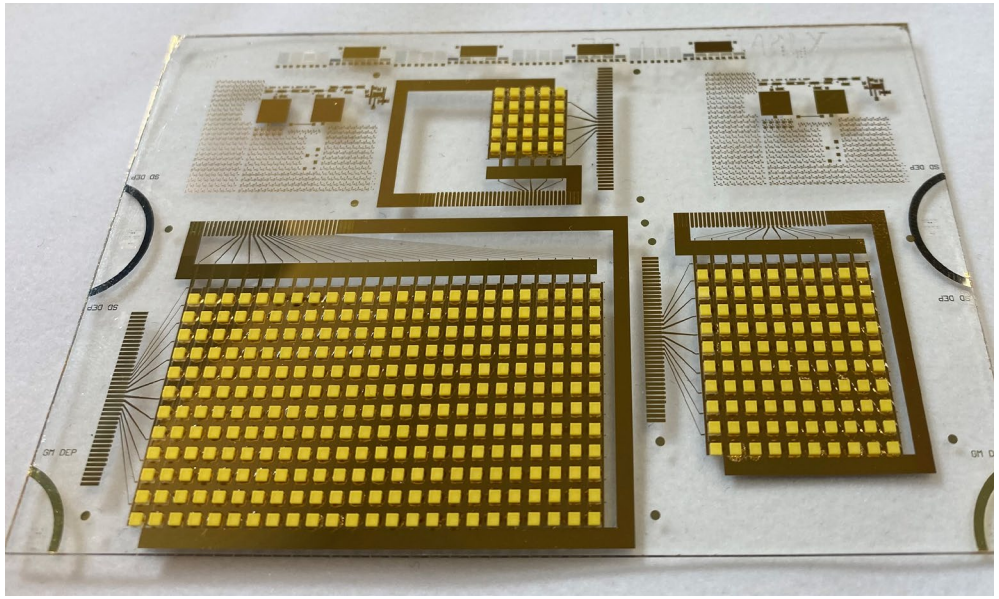
# Mini LED backlights

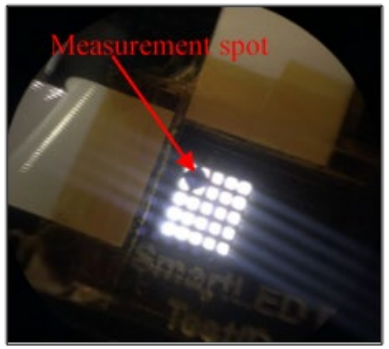
- LEDs attached to OTFT backplane using pick-and-place
- Flexible connectors tab bonded to custom driver electronics



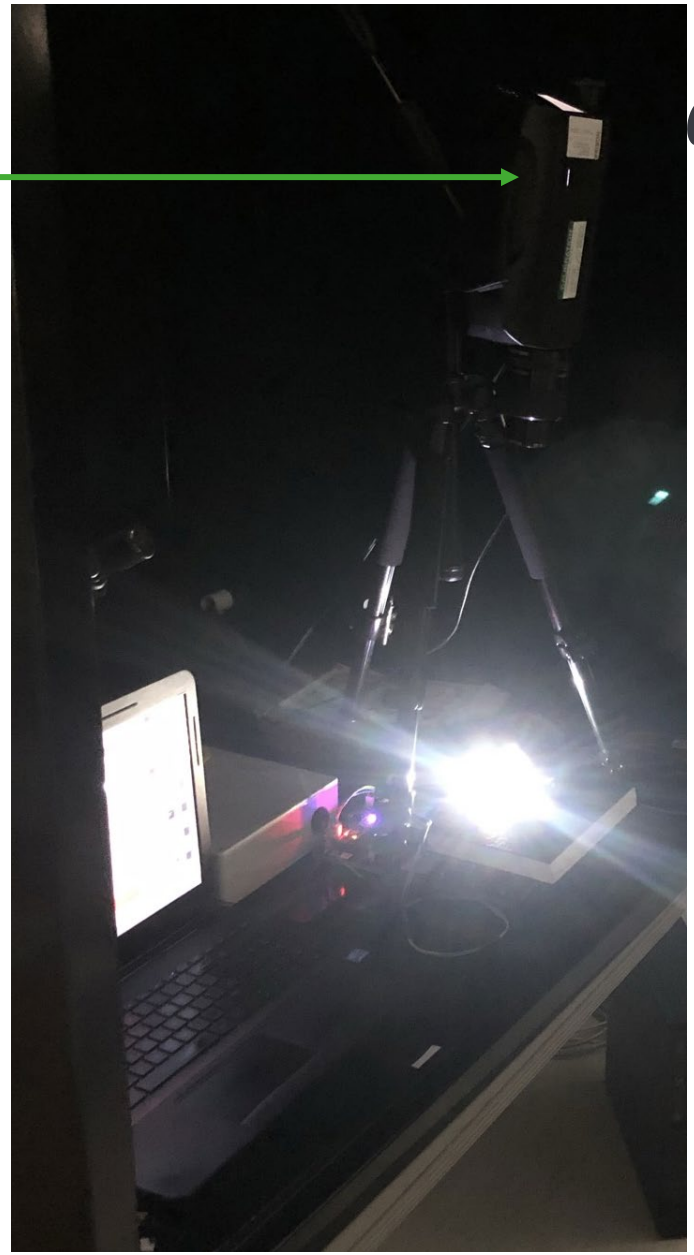


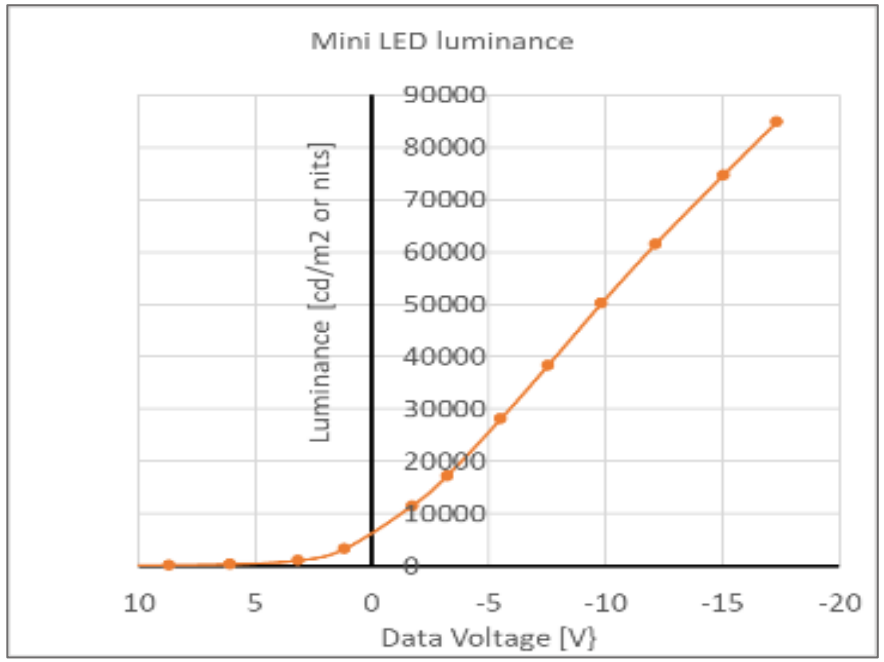
# Backlight luminance testing

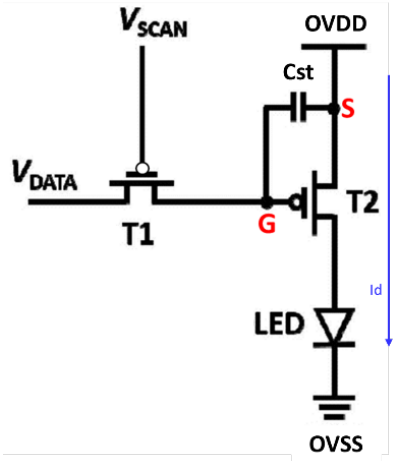



Spectrascan
PR670



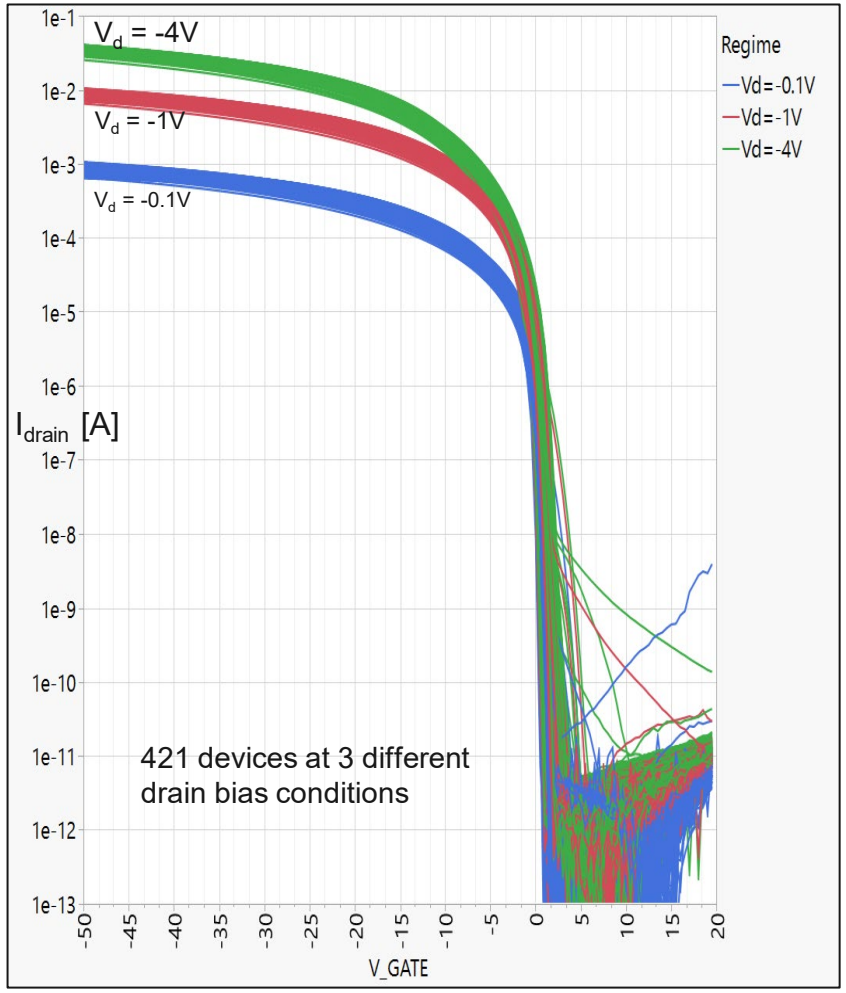
$V_{dd}$ to $V_{ss}$ = +8.6 V
$V_{select}$ +24V to -24V
$V_{data}$ vs Luminance measured



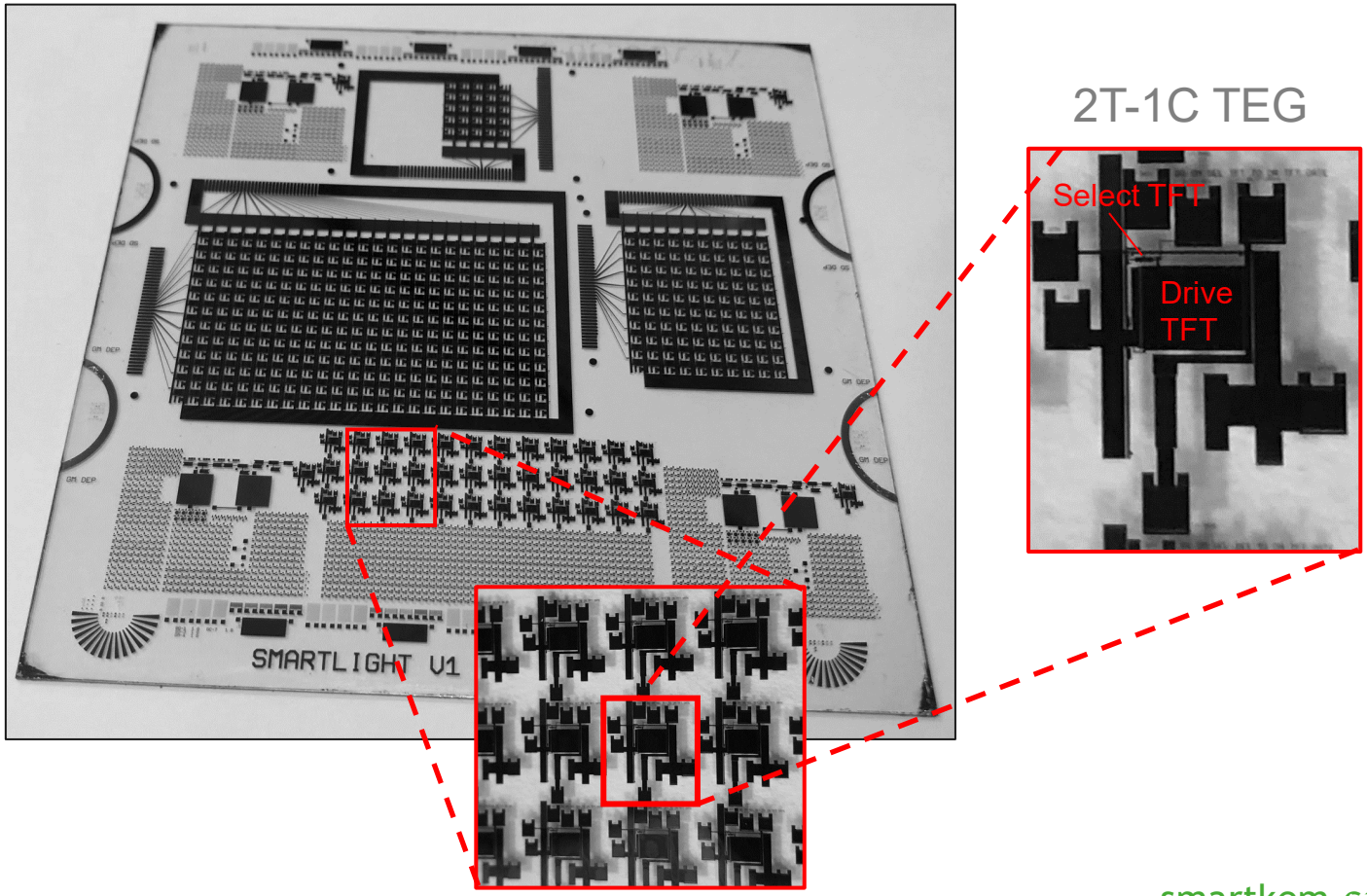




Measured 85,000 nits – equates to 4250 nits front of screen with a 5% transmission through LCD and a contrast ratio of 1,000,000:1 if the LCD has a native contrast ratio of 2000:1

# Electrical Performance of TRUFLEX™ OTFT array



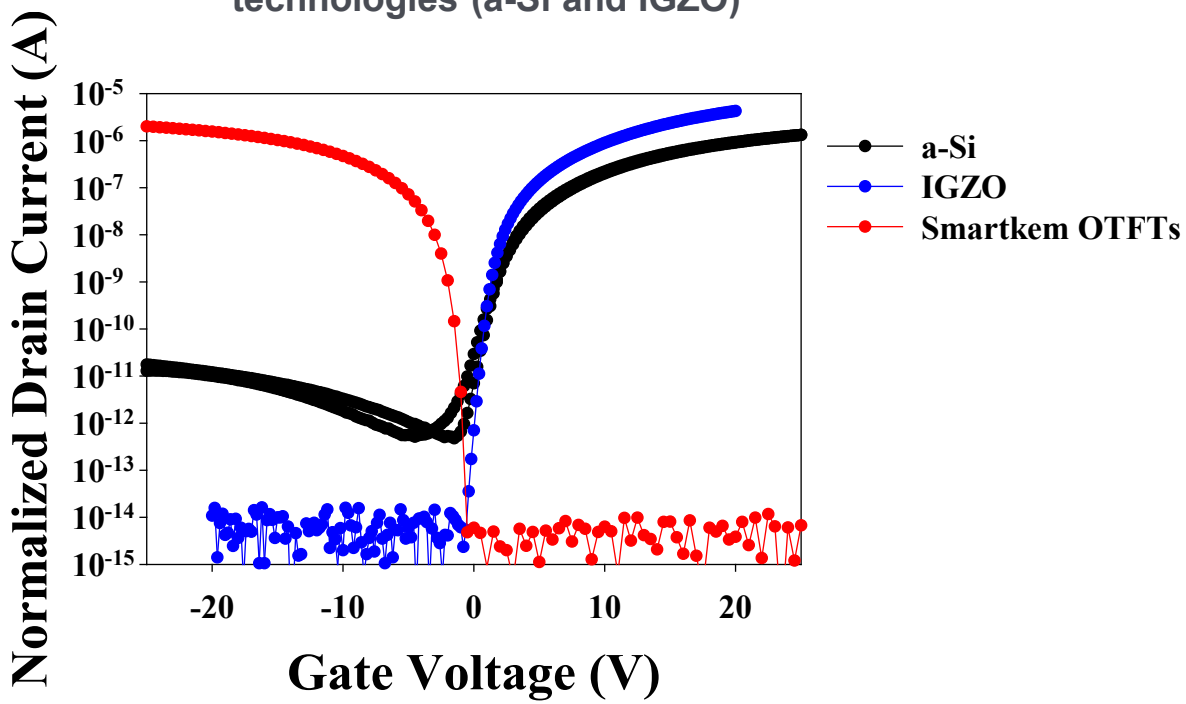

- 40mA median on current, $V_d$ = -4,V $V_g$ = -50V
- Off current is a few pA
- On/off ratio is ~$10^{10}$



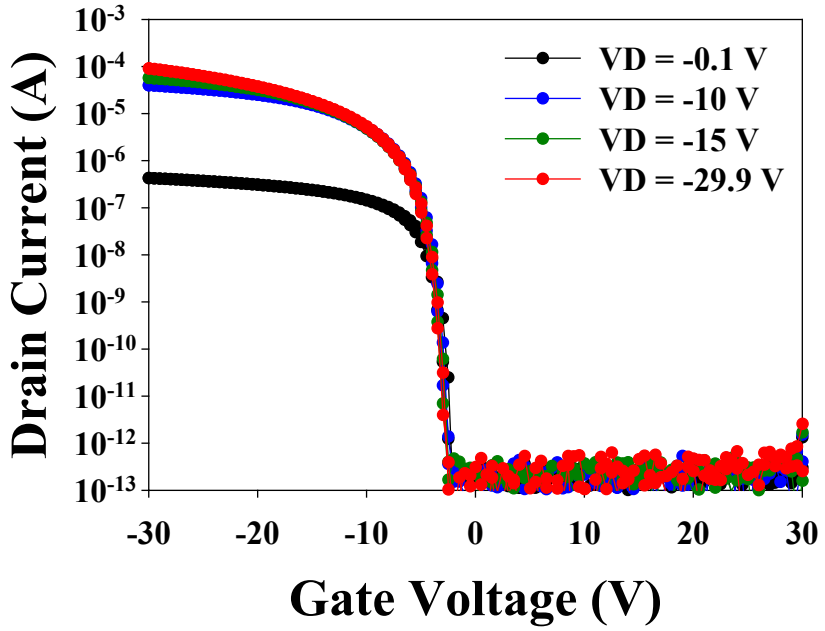
# Comparison of TFT characteristics

- OTFTs offer a low-off current level for VGL switch benefits vs a-Si
- OTFT is capable of high voltage stability in driving (for bi-stable display applications)

**SmartKem vs. other large area TFT technologies (a-Si and IGZO)**

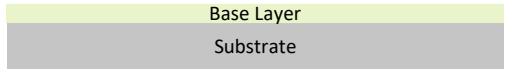



**SmartKem Voltage Turn-on Stability**



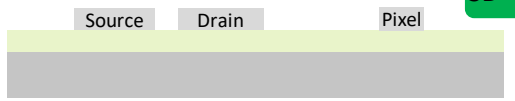
# TruFlex Stack - OTFT process

Substrate with suitable interfacial layer

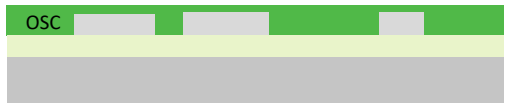



Sputtered Source/drain deposition

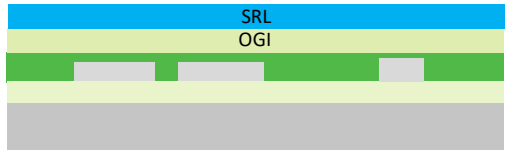
SD – Mask 1




OSC deposition (spin coat/slot die)

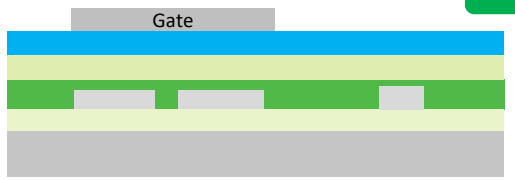



OGI & SRL deposition (spin coat/slot die)

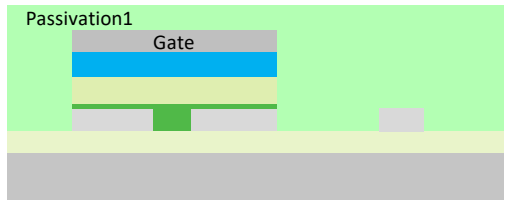



Sputtered Gate deposition and pattern

G – Mask 2



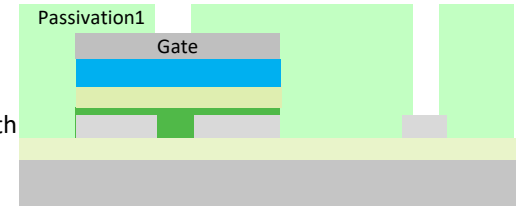

Dry etch OGI and OSC




Passivation1 deposition (spin coat/slot die)

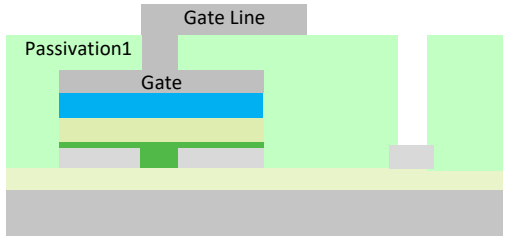
Passivation1 photolith and realise via

PV1 – Mask 3



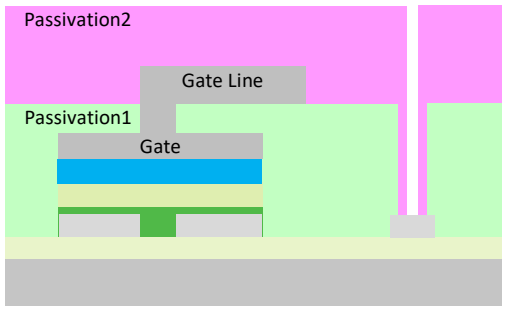

Sputtering Gate contact deposition and pattern

GC – Mask 4




Passivation1 deposition (spin coat/slot die)

PV2 – Mask 5




Passivation2 photolith and realise via

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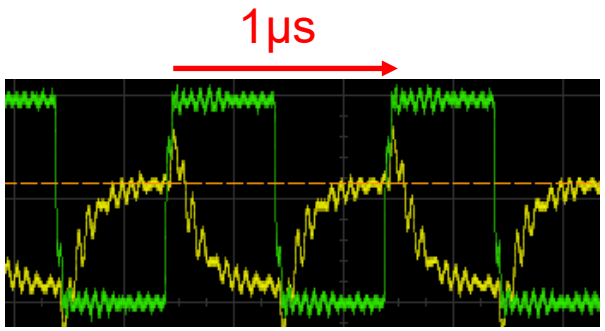
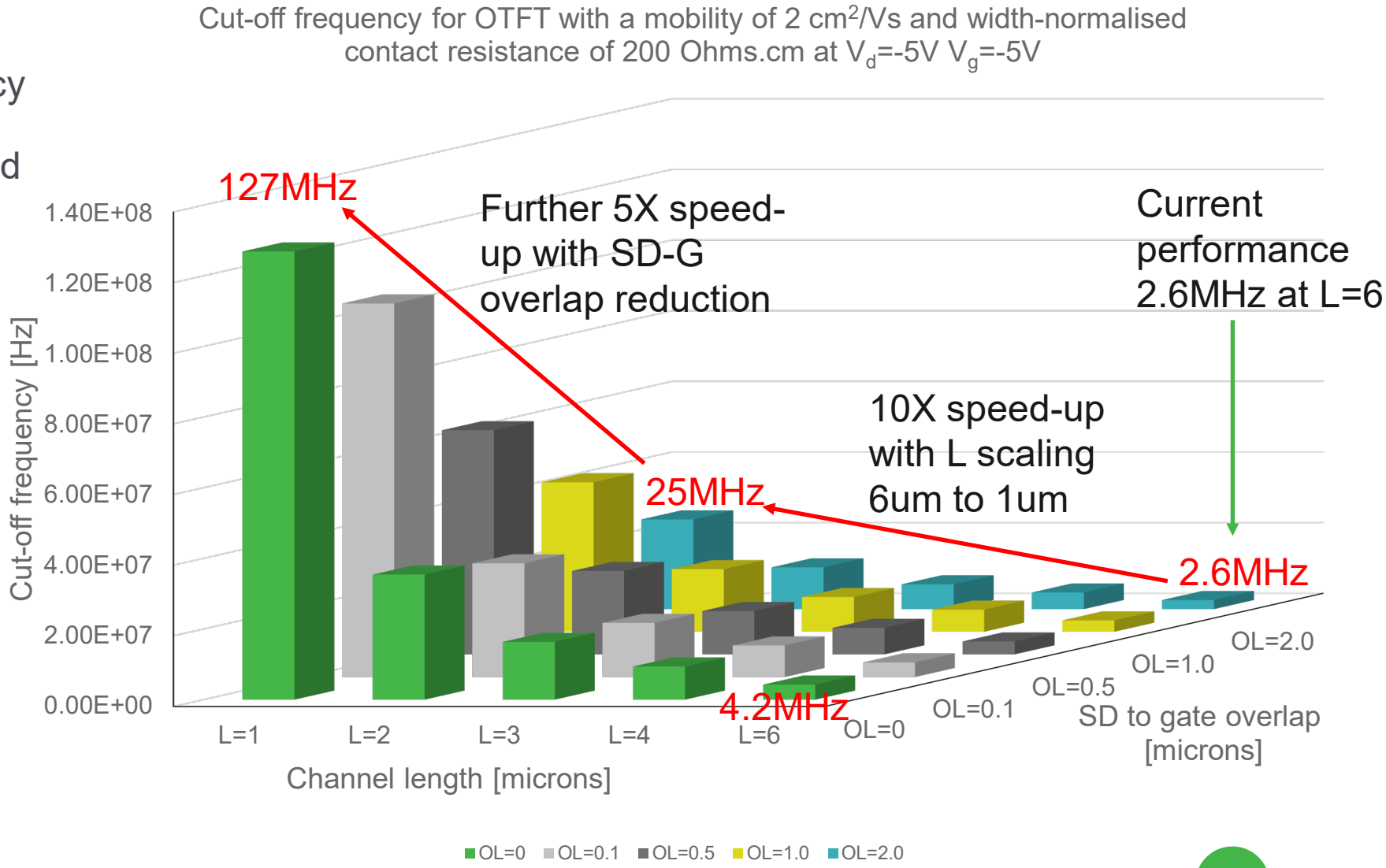
# SmartKem OTFT for digital logic

- PMOS only transistors
- Single transistor cut-off frequency $f_T$ is ~2.6MHz for devices with minimum overlap of 2 micron and L=6 µm (after wet etching) – matches with test data




- With channel length scaling to 1 micron $f_T$ will increase to 25MHz
- Using a self-aligned process for L=1µm OTFT $f_T$ would reach ~127MHz

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# You need an ecosystem for success

1
Organic INKS

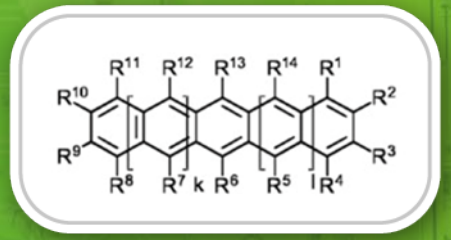
2
Design Tools

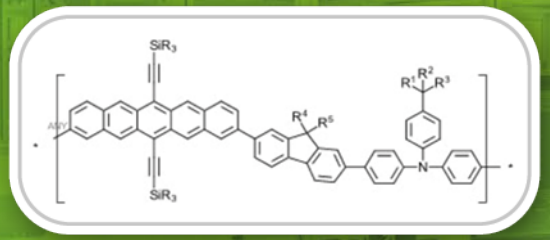
3
Foundry Services

**Mass Deployment**

# 1. TRUFLEX® Inks – Available at Scale

## Components of TRUFLEX® Inks





### High Mobility, Small Molecule

- Intrinsic mobility ≥ 10 $cm^2/Vs$

### Semiconducting Polymer 'Controls'

- Morphology of OSC layer
- Phase segregation & uniformity of SM
- Viscosity of ink

### Solvents

- Solubilise SM & Binder
- Modify surface tension
- Influence ink viscosity
- Customise for range of printing methods

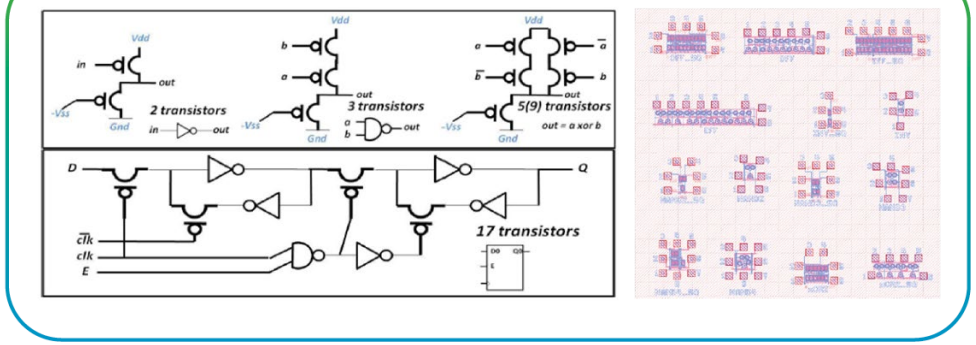
- Technical team has excellent understanding of formulations
- In-depth knowledge of how to combine small molecule/semiconducting polymer to maximise the performance of OSC layer and resulting oTFT
- More than 50 years expertise relating to OSC formulation

- Best in class performance
- Compatible with existing a-Si process lines
- Scaled up manufacture

# 2. TRUFLEX® Electronic Design Automation Tools - In Development

## EDA Components to Libraries

| Device | PCell name | Design parameters | Symbol | Layout |
|---|---|---|---|---|
| Resistor | rlin_lw<br>rlin_rw | w strip width<br>l strip length / r resistance | | |
| | rsnake_lwz<br>rsnake_rwz | w strip width<br>z meanders number<br>l vertical bars length / r resistance | | |
| Capacitor | cap_lw<br>cap_cw | w upper plate width<br>l upper platelength / c capacitance | | |
| Inductor | indsq_srwnt | s turns spacing<br>r interior turn radius<br>w turns width<br>nt number turns | | |
| | indoct_srwnt | s turns spacing<br>r interior turn radius<br>w turns width<br>nt number turns | | |
| Diode | diode_lw | l upper contact length<br>w upper contact width | | |
| Transistor | potft_wl | l channel length<br>w channel width | | |




- EDA tools establishment
- PDK (Process Design Kit) establishment (at PE foundries)
  - Standard cells – parameterizable cells (p-cells)
  - Libraries of circuits and other PE devices (force sensor, OLED, OPD, biosensor etc)
  -

# 3. TRUFLEX® Foundry Services

**CPI Prototyping facility for materials qualification, process development & fabrication**

**Adding digital lithography** for full-custom circuits - sheet to sheet initially and then **roll-to-roll** in the future

# Moore’s Law

- **Moore’s law is the observation that the number of transistor in a dense integrated circuit (IC) doubles about every two years. It is an observation and projection of an historical trend. Rather than a law of physics, it is an empirical relationship linked to gains from experience in production.**