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Microchip Enters Memory Infrastructure Market with Serial Memory Controller for High-performance Data Center Computing

SMC 1000 8x25G enables high memory bandwidth required by next-generation CPUs and SoCs for AI and machine learning

CHANDLER, Ariz., Aug. 5, 2019 /PRNewswire/ -- As the computational demands of artificial intelligence (AI) and machine learning workloads accelerate, traditional parallel attached DRAM memory has presented a major roadblock for next-generation CPUs, which require an increased number of memory channels to deliver more memory bandwidth. Microchip Technology Inc. (Nasdaq: MCHP) today announced an expanded data center portfolio and its entrance into the memory infrastructure market with the industry's first commercially available serial memory controller. The **SMC 1000 8x25G** enables CPUs and other compute-centric SoCs to utilize four times the memory channels of parallel attached DDR4 DRAM within the same package footprint. Microchip's serial memory controllers deliver higher memory bandwidth and media independence to these compute-intensive platforms with ultra-low latency.

As the number of processing cores within CPUs has risen, the average memory bandwidth available to each processing core has decreased because CPU and SoC devices cannot scale the number of parallel DDR interfaces on a single chip to meet the needs of the increasing core count. The SMC 1000 8x25G interfaces to the CPU via 8-bit Open Memory Interface (OMI)-compliant 25 Gbps lanes and bridges to memory via a 72-bit DDR4 3200 interface. The result is a significant reduction in the required number of host CPU or SoC

pins per DDR4 memory channel, allowing for more memory channels and increasing the memory bandwidth available.

A CPU or SoC with OMI support can utilize a broad set of media types with different cost, power and performance metrics without having to integrate a unique memory controller for each type. In contrast, CPU and SoC memory interfaces today are typically locked to specific DDR interface protocols, such as DDR4, at specific interface rates. The SMC 1000 8x25G is the first memory infrastructure product in Microchip's portfolio that enables the media-independent OMI interface.

Data center application workloads require OMI-based DDIMM memory products to deliver the same high-performance bandwidth and low latency results of today's parallel-DDR based memory products. Microchip's SMC 1000 8x25G features an innovative low latency design that delivers less than four ns incremental latency over a traditional integrated DDR controller with LRDIMM. This results in OMI-based DDIMM products having virtually identical bandwidth and latency performance to comparable LRDIMM products.

"Microchip is excited to introduce the industry's first serial memory controller device to the market," said Pete Hazen, vice president of Microchip's Data Center Solutions business unit. "New memory interface technologies such as Open Memory Interface (OMI) enable a broad range of SoC applications to support the increasing memory requirements of high-performance data center applications. Microchip's entrance into the memory infrastructure market underscores our commitment to improving performance and efficiency in the data center."

"IBM customer workload requirements are increasingly memory-intensive, which is why we have made the strategic decision for POWER processor memory interfaces to utilize OMI standard interfaces to increase memory bandwidth," said Steve Fields, chief architect of IBM Power Systems. "IBM appreciates the partnership with Microchip to deliver this solution."

SMART Modular, Micron and Samsung Electronics are building multiple pin-efficient 84-pin Differential Dual-Inline Memory Modules (DDIMM) with capacities ranging from 16 GB to 256 GB, conforming to the draft JEDEC DDR5 standard DDIMM form factor. These DDIMMs will leverage the SMC 1000 8x25G and will seamlessly plug into any OMI-compliant 25 Gbps interface.

Quotes
"The Open Memory Interface (OMI) standard delivers a pin-efficient serial memory interface so a broad range of CPU and SoC applications can both scale memory bandwidth and seamlessly transition between an increasing number of emerging media types such as storage class memory," said Myron Slota, president of the OpenCAPI Consortium. "The OpenCAPI consortium provides royalty-free host and target IP, as well as drives a broad set of initiatives to ensure standards compliance."

"Google customers benefit from data intensive applications such as machine learning and data analytics that require high performance memory," says Rob Sprinkle, technical lead for platforms infrastructure at Google LLC. "Google strongly supports open standards-based initiatives such as the Open Memory Interface (OMI), which provides a high-performance memory interface to meet these important bandwidth and latency performance goals."

Development Tools
To support customers building systems that are compliant with the OMI standard, the SMC

1000 comes with design-in collateral and ChipLink diagnostic tools that provide extensive debug, diagnostics, configuration and analysts tools with an intuitive GUI.

Pricing and Availability
The SMC 1000 8x25G is sampling now. For additional information, visit: **https://www.microchip.com/smartmemory.**

To order samples, contact a Microchip sales representative.

Resources
High-res images available through Flickr or editorial contact (feel free to publish):

- Application image: **https://www.flickr.com/photos/microchiptechnology/48417967966**
- Video: **https://www.youtube.com/watch?v=vo4XUZ8dNgI&feature=youtu.be**

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