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# Microchip Unveils Industry's First Terabit-Scale Secure Ethernet PHY Family with Port Aggregation for Enterprise and Cloud Interconnect

## META-DX2+ enables OEMs to double router and switch system capacities with 112G PAM4 connectivity for 800G ports, adds encryption and Class C/D precision timing

CHANDLER, Ariz., Sept. 19, 2022 (GLOBE NEWSWIRE) -- The demand for increased bandwidth and security in network infrastructure driven by growth in hybrid work and geographical distribution of networks is redefining borderless networking. Led by AI/ML applications, the total port bandwidth for 400G (gigabits per second) and 800G is forecasted to grow at an annual rate of over 50%, according to 650 Group. This dramatic growth is expanding the transition to 112G PAM4 connectivity beyond just cloud data center and telecom service provider switches and routers to enterprise Ethernet switching platforms. Microchip Technology Inc. (NASDAQ: MCHP) is responding to this market inflection with the **META-DX2 Ethernet PHY** (physical layer) portfolio by introducing a new family of META-DX2+ PHYs. These are the industry's first solution set to integrate 1.6T (terabits per second) of line-rate end-to-end encryption and port aggregation to maintain the most compact footprint in the transition to 112G PAM4 connectivity for enterprise Ethernet switches, security appliances, cloud interconnect routers and optical transport systems.

"The introduction of four new META-DX2+ Ethernet PHYs demonstrates our commitment to supporting the industry transition to 112G PAM4 connectivity powered by our META-DX retimer and PHY portfolio. In conjunction with our META-DX2L retimer, we now offer a complete chipset for all connectivity needs from retiming, gearboxing, to advanced PHY functionality," said Babak Samimi, corporate vice president of Microchip's communications business unit. "By offering both hardware and software footprint compatibility, our customers can leverage architectural designs across their enterprise, data center, and service provider switching and routing systems that can offer pay-as-you-need enablement of advanced features including end-to-end security, multi-rate port aggregation, and precision timestamping via a software subscription model."

The META-DX2+'s configurable 1.6T datapath architecture outperforms the next near competitors by 2x in total gearbox capacity and hitless 2:1 protection switch mux modes enabled by its unique ShiftIO capability. The flexible XpandIO port aggregation capabilities optimize router/switch port utilization when supporting low-rate traffic. Also, the devices include IEEE 1588 Class C/D Precision Time Protocol (PTP) support for accurate nanosecond timestamping required for 5G and enterprise business critical services. By offering a portfolio of footprint-compatible retimer and advanced PHYs with encryption

options, Microchip enables developers to expand their designs to add MACsec and IPsec based on a common board design and Software Development Kit (SDK).

META-DX2+ differentiated capabilities include:

- Dual 800 GbE, quad 400 GbE and 16x 100/50/25/10/1 GbE MAC/PHY
- Integrated 1.6T MACsec/IPsec engines that offload encryption from packet processors so systems can more easily scale up to higher bandwidths with end-to-end security
- Greater than 20% board savings compared to competing solutions that require two devices to deliver the same 1.6T gearbox and hitless 2:1 mux modes
- XpandIO enables port aggregation of low-rate Ethernet clients over higher speed Ethernet interfaces, optimized for enterprise platforms
- ShiftIO feature combined with a highly configurable integrated crosspoint enables flexible connectivity between external switches, processors, and optics
- Device variants with 48 or 32 Long Reach (LR) capable 112G PAM4 SerDes including programmability to optimize power vs. performance
- Support for Ethernet, OTN, Fibre Channel and proprietary data rates for AI/ML applications

“As the industry transitions to a 112G PAM4 serial ecosystem for high-density routers and switches, line-rate encryption and efficient use of port capacity becomes increasingly important,” said Alan Weckel, founder and technology analyst at 650 Group, LLC. “Microchip’s META-DX2+ family will play an important role in enabling MACsec and IPsec encryption, optimizing port capacity with port aggregation, and flexibly connecting routing/switching silicon to multi-rate 400G and 800G optics.”

Like the META-DX2L retimer, the new series of META-DX2+ PHYs can be used with Microchip’s PolarFire® FPGAs, the ZL30632 high-performance PLL, oscillators, voltage regulators, and other components that have been pre-validated as a system to help speed designs into production.

**Development Tools**

Microchip’s second-generation Ethernet PHY SDK for the META-DX2 family lowers development costs with field-proven API libraries and firmware. The SDK supports all META-DX2L and META-DX2+ PHY devices within the product family. Support for the Open Compute Project (OCP) Switch Abstraction Interface (SAI) PHY extensions are included to enable agnostic support of the META-DX2 PHYs within a wide range of Network Operating Systems (NOS) that support SAI.

**Availability**

The META-DX2+ family is expected to sample during the fourth calendar quarter of 2022. For additional information visit the **META-DX2+ webpage** or contact a Microchip sales representative.

**See the META-DX2L Ethernet PHY at ECOC 2022**

Microchip will be exhibiting the META-DX2L PHY device, which started sampling in the fourth quarter of 2021, in the Optical Internetworking Forum (OIF) booth at the European Conference on Optical Communication (ECOC) September 18-22, 2022, in Basel Switzerland. Microchip and other OIF members will be showcasing how multi-vendor

interoperability is accelerating industry solutions for the global network in booth #701 at the Congress Center Basel.

## Resources

High-res images available through Flickr or editorial contact (feel free to publish):
• Application image: **www.flickr.com/photos/microchiptechnology/52336953308/sizes/l/**

## About Microchip Technology

Microchip Technology Inc. is a leading provider of smart, connected and secure embedded control solutions. Its easy-to-use development tools and comprehensive product portfolio enable customers to create optimal designs which reduce risk while lowering total system cost and time to market. The company solutions serve more than 120,000 customers across the industrial, automotive, consumer, aerospace and defense, communications and computing markets. Headquartered in Chandler, Arizona, Microchip offers outstanding technical support along with dependable delivery and quality. For more information, visit the Microchip website at www.microchip.com.

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